DEVELOPMENT OF MICROMACHINED MILLIMETER WAVE MODULES FOR WIRELESS COMMUNICATION SYSTEMS

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DEVELOPMENT OF MICROMACHINED MILLIMETER WAVE MODULES FOR WIRELESS COMMUNICATION SYSTEMS

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To my beloved family

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SUMMARY

This research discusses the design, fabrication, integration, and characterization of micromachined millimeter-wave components and a signal source for submillimeter-wave multiplier source using the deep reactive ion etching technique. A wide range of micromachined millimeter-wave components are presented in this thesis. Micromachined low-loss straight and meander waveguides from 75 GHz to 110 GHz are reported first. The tolerances of a micromachined straight waveguide are analyzed.

Next, a micromachined W-band bandpass filter is introduced. The three-pole Chebyscheff bandpass filter has 0.5-dB ripples in the passband and at least 30-dB attenuation at 9 GHz away from the center frequency. The passband insertion loss is only 1.1 dB to 1.3 dB with a bandwidth of 4.83%. Then, a W-band hybrid coupler and a W-band power divider are presented. The hybrid coupler and the power divider are designed in the H-plane of a rectangular waveguide. The hybrid coupler uses a ridged waveguide 90° phase shifter to reduce phase deviation and a joint waveguide to achieve a broad bandwidth. The power divider employs a T-shape topology. The measured response presented in this work shows good agreement with simulated response. The power divider and the hybrid coupler cascade, and a measured combining efficiency is reported.

The next two chapters demonstrate a novel micromachined wideband transition from a coplanar waveguide (CPW) to a rectangular waveguide (RWG) from 75 GHz to 110 GHz and a waveguide filter taking full advantage of this transition. The comprehensive analysis of the transition and the study on parameters are given in detail. In the proposed filter design, metal-coated probes are used to couple signals

from CPW lines to cavity-based resonators. The waveguide-based input and output ports are no longer needed. This design significantly reduces the size of the filter. The measured response has a center frequency of 96.6 GHz, a bandwidth of 2.9%, and a passband insertion loss of 4.14 dB. Chapter 7 introduces a high quality factor (high-Q) tunable cavity resonator. This proposed design tackles the problem of using planar element to tune the resonance of a 3-D cavity resonator. Therefore, reconfigurable cavity-based components are enabled by the proposed tunable resonator for wireless communication systems.

The second topic of this thesis investigates the signal generation at submillimeter-wave frequency range. A wideband 900 GHz frequency multiplier is designed, implemented, and integrated in a micromachined waveguide structure. The input signals are generated by a 300 GHz tripler and coupled to a suspend microstrip line that supports the propagation in a TEM mode through an E-plane probe. The generated third harmonic signals are coupled to an output waveguide through the output E-plane probe. The design, simulation, fabrication, and measurement of the 900 GHz frequency multiplier are presented in detail.

CHAPTER I

INTRODUCTION

1.1 Motivation

For several decades, millimeter-wave technologies in wireless communication systems have been extensively investigated. The increasing demand for high data rate wireless transmissions, predicted by the international technology roadmap for semiconductors (ITRS) [1], requires a high carrier frequency for emerging applications due to the radio frequency congestion at the low-frequency end and a large amount of unused bandwidth in the millimeter-wave spectrum. In the United States and several other countries, up to 7-GHz unlicensed bandwidth around 60 GHz is dedicated to high-speed multimedia data transmissions, which are known as wireless personal area networks [2]. Figure 1 shows the IBM 60-GHz transceiver, which provides a high data rate on the level of Gbps [2]. This transceiver can benefit many high data rate applications, including wireless HDTV, wireless USB 2.0, and wireless gigabit Ethernet. Another application of millimeter-wave techniques is a 77-GHz anti-collision system that has been proposed to improve the driving safety of automobiles using millimeter-wave radar systems [3]. In addition, weather radar and imaging applications at 94 GHz have been introduced to enhance landing safety and security [4].

One of the most scientifically valuable spectrum regions is the submillimeter-wave band, or the terahertz (THz) band, spanning from 100 GHz to 10 THz. However, it is the least explored frequency band due to the lack of robust technologies [5]. The universe is naturally bathed in THz radiation that peaks at 3 THz. THz radiation mostly passes unnoticed and undetected. The THz signals contain a great deal of information about remote areas far from the earth. Among the abundant amount of

information, the dynamic properties of a wide range of molecules in remote regions are hidden. The structures of molecules can be studied through the observation of molecule resonances. Furthermore, the unique properties of THz signals enable many applications in radio astronomy, plasma fusion diagnostics, atmospheric earth observation, molecular spectroscopy, and high-resolution imaging. In the application of atmospheric earth observation, the investigation of the correlation between the shape of the ozone hole and the distribution of chlorine monoxide tackles the puzzle of how human activities affect the health of our planet. Figure 2 presents an image taken by the submillimeter-wave instrument on a NASA satellite of the ozone hole over Antarctica in 2004 [6].

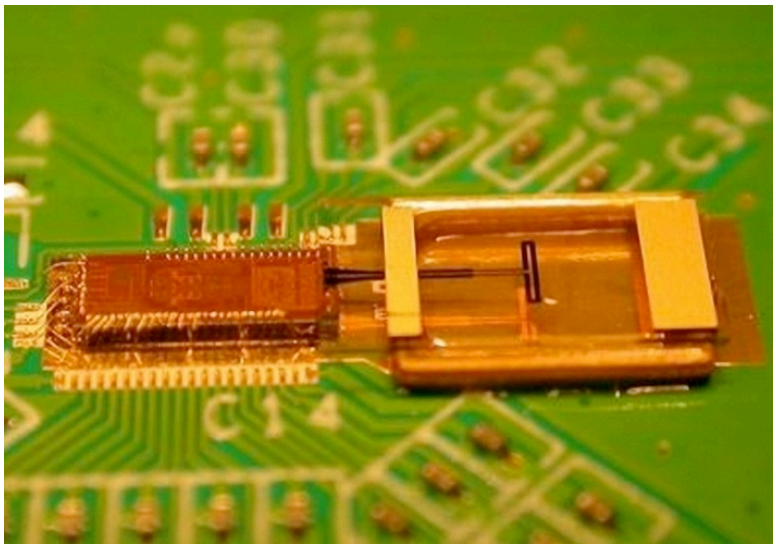


Figure 1: The IBM 60 GHz transceiver [2].

1.2 Background

Until the early 1980's, most of the millimeter-wave components were fabricated using waveguide passives. Waveguide passives are low loss, high power capacity, and high quality factor, but they are bulky and heavy for applications that have stringent size and weight requirements. Furthermore, the conventional machining cost of waveguide

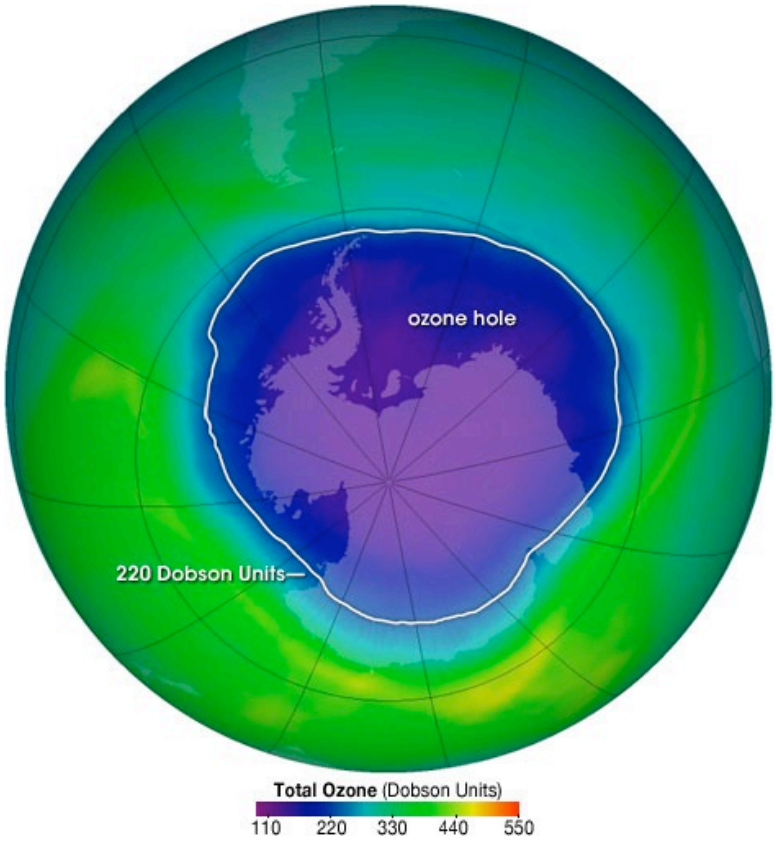


Figure 2: The ozone hole on 4 October 2004 as measured by the ozone monitoring instrument on the Aura satellite. Values are in Dobson units. The edge of the hole is defined by the 220 Dobson unit contour [6].

passives is becoming extremely prohibitive when the operating frequency is in the THz band and the wavelength is in the submillimeter range. Different from the conventional machining technique, micromachining techniques, including photolithography, etching, and film deposition, originally developed in the semiconductor industry, were pioneered by research groups at the University of Michigan and Caltech two decades ago to achieve good performance in the millimeter-wave frequency range [7]. Micromachining techniques are capable of improving the performance and lowering the cost of millimeter-wave and submillimeter-wave components.

Two types of micromachined passives, planar passives and three-dimension (3-D) passives, have been extensively studied in the literature [8]. Planar passives, using

either a microstrip or a coplanar waveguide, have been widely used in millimeter-wave circuits. The performance of planar passives inevitably deteriorates with increased operating frequencies because of frequency dispersion, substrate dependence, and dielectric loss that is approximately propotional to operating frequencies. Micromachined planar passives with reduced dielectric loss have been enabled by the following approaches:

- Having membrane-supported components with reduced effective dielectric constants by partially removing a substrate [9] [10], shown in Figure 3.
- Elevating planar circuits in the air [11].
- Adding a low-loss, low dielectric constant (low-k) layer between circuits and high dielectric constant substrates [12] [13].
- Reducing the dielectric constant of a substrate using chemical reactions [14].

Micromachined planar circuits with reduced conductor loss are enabled by either an electroplating technique [15] [16] or a high-temperature superconductor (HTS) [17] [18]. The electroplating technique that changes the geometry of planar transmission lines is effective at reducing conductor loss, especially when the skin depth at operating frequencies is close to the thickness of the transmission lines. HTS, discovered in 1911 with hundreds of variations, has a fabrication process that is compatible with monolithic microwave circuits. The most widely-used HTS films are the yttrium barium copper oxide (YBCO) film and the thallium barium calcium copper oxide (TBCCO) film [19] [20].

With the micromachined techniques discussed above, many planar millimeter-wave components have been reported with enhanced performance. In [21], a patch antenna on a membrane-supported substrate was characterized. The bandwidth of the antenna was increased by 64%, and the efficiency was increased by as much as

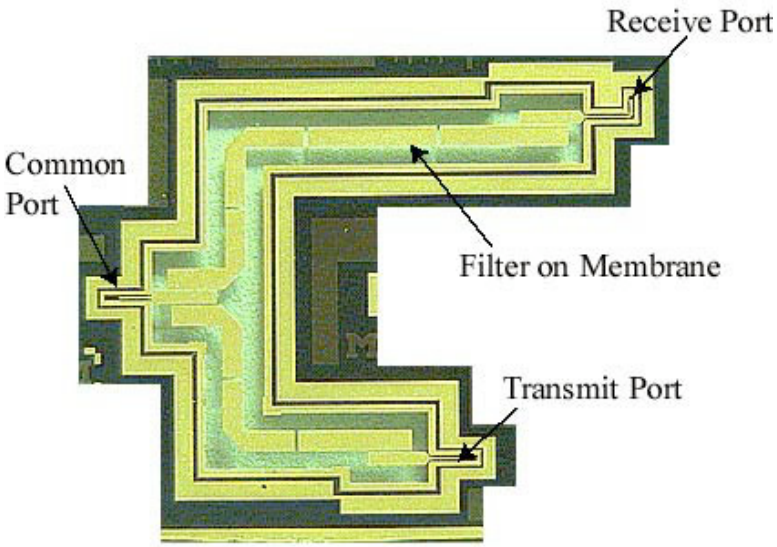


Figure 3: The membrane supported planar passive [8].

28%. In [22], a W-band five-section bandpass filter showed a passband insertion loss of 3.6 dB with a bandwidth of 6.1%. The circuits of the filter were fabricated on top of a dielectric membrane and assembled in a shielded membrane microstrip structure. In [23], an elevated CPW line was fabricated by removing the silicon between the signal line and the ground planes. The attenuation was improved by more than 20%. In [11], a coupler was introduced to cover the frequency range from 15 GHz to 45 GHz, shown in Figure 4. The frequency dispersion of the coulper were significantly reduced by elevating the lines in the air. In [24], the low dielectric constant and low-loss materials were applied on top of a silicon substrate to reduce the effective dielectric constant of planar transmission lines. A 10-μm thick polymer layer was used to reduce the effective dielectric constant. Thus, a 50% reduction of insertion loss was achieved with the increased quality factor by 30%−50%. In [14], a 50-μm deep trench was etched on silicon and filled with silicon dioxide using a low-pressure chemical vapor deposition process, and finite ground coplanar waveguide lines were fabricated on top of the trenches. Measured results of the waveguide lines showed an attenuation of 1.5 dB/cm at 20 GHz. The low attenuation came from increased

substrate resistivity and decreased effective dielectric constant.

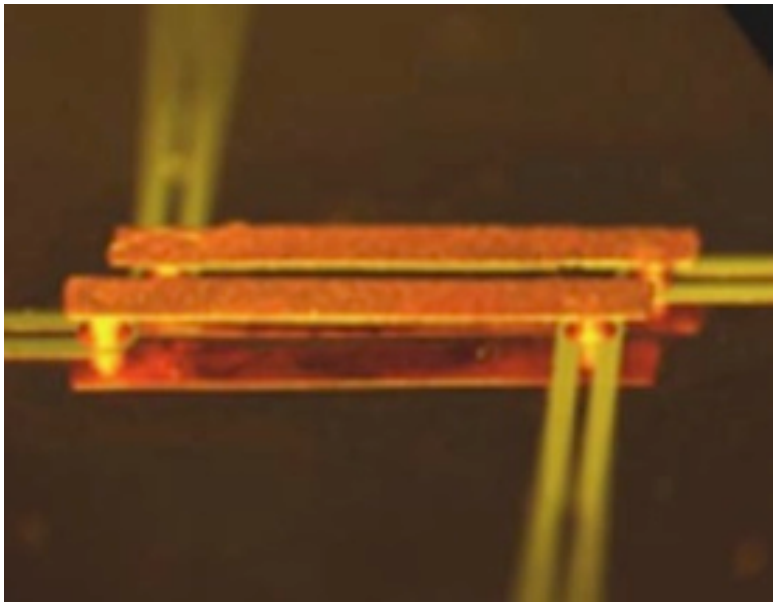


Figure 4: The elevated planar passive [11].

Micromachined 3-D passives have attracted considerable attention recently due to their intrinsic superior quality factors over planar passives. Advanced micromachining techniques have made these 3-D circuits feasible in the millimeter and submillimeter-wave frequency ranges. Micromachined 3-D circuits with high precision are critical for the delivery of affordable and high-performance submillimeter-wave components. Micromachining techniques for 3-D components include the following approaches:

- The via-based multilayer technique
- The sterero-lithography technique
- The surface micromachining technique
- The laser-based etching technique
- The bulk micromachining technique

The via-based multilayer technique has been widely used in substrate integrated waveguides (SIW) [25] [26] and multilayer LTCC components [27] [28]. Despite its

advantages of compact size and easy integration with planar circuits, the substrate-dependent via-based components have a loss tangent and a dielectric constant associated directly with laminated dielectric filling. Many SIW-based passives, such as a transition from a planar waveguide to a SIW line, were reported in [25]. In [27] [28], multilayer LTCC-based filters and antenna were presented at 60 GHz with good measured responses.

The stereo-lithography method is a 3-D fabrication method that has been extensively studied by research groups from the University of Michigan and Purdue University [107] [108]. This method scans and cures the photo-curable monomer with laser beams layer by layer. The drawback of this method is that the fabrication is not compatible with the standard CMOS process. The stereo-lithography method is suitable for stand-alone components instead of monolithic integrated circuits because the entire structure is immersed in resin.

The surface micromachining technique is a substrate-independent process using film deposition. The photo-definable polymer in the film deposition is employed as a structure or sacrificial layer. The height of a structure or sacrificial layer varies from less than 1 micron to hundreds of microns, depending on the viscosity of polymers, the spin speed, and the curing condition. RF MEMS switches [31] [32], including both cantilever and capacitive types, are examples of surface micromachined components. Another example is the use of negative photo-definable polymers, e.g., SU-8, to build photo-defined 3-D structures up to 2 mm with a high aspect ratio [34]. The SU-8 pillars are used to replace solid metal sidewalls of cavities with metal-coated fences. Several 60-GHz millimeter-wave components and a front-end transceiver using the SU-8 pillar fence technique were presented in [36] [37] with the good agreement between the theoretical analysis and the experimental results. The limit of this technique is complicated fabrication processes.

The laser beam etching technique has been proposed to drive silicon etching using

chemical reactions. A laser-assisted chemical etching system is summarized in [38]. The Cl_2 gas is used to accelerate the etching process. The laser beam etching can achieve complicated 3-D structures in a small area. In [111], a laser-etched feedhorn structure on silicon was presented. The laser beam etching technique is very useful for THz components operating above 500 GHz. Figure 5 shows a 2-THz waveguide structure fabricated using the laser beam chemical etching technique at the University of Arizona.

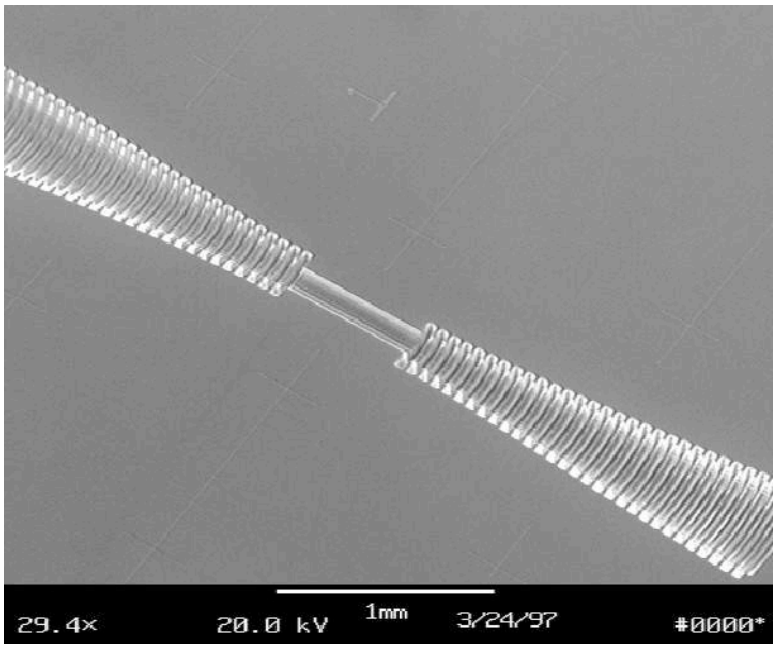


Figure 5: The SEM photo of a 2-THz waveguide structure using the laser chemical etching technique [111].

Two bulk silicon micromachining techniques, wet etching and dry etching, have been extensively investigated and reported in [38] [111]. For wet etching, many chemicals are commercially available. The selection of an etchant depends on the type of etching, the properties of a material, the material of masks, and its compatibility with existing circuits. Two types of wet etching are isotropic wet etching and anisotropic wet etching. In isotropic wet etching, etching speeds are almost the same in all directions. One type of isotropic etchant is HNA, which consists of hydrofluoric acid,

nitric acid, and acetic acid. A layer of silicon dioxide or silicon nitride is typically used as the mask layer of this type of etchant. Different from isotropic silicon etching, anisotropic silicon etching is commonly used in micromachining techniques. In anisotropic silicon etching, the etching speed depends on the crystallographic direction. For this reason, it is called orientation-dependent etching. The etching rate on the <111> plane of silicon wafers is remarkably slower than that on the other planes. Eventually, the <111> plane that has the slowest etching rate is exposed. When two wet-etched silicon samples bond, a waveguide structure [38] can form. One of the widely used chemicals for anisotropic etching is KOH, a hydroxide of alkali metal. KOH etching can result in a very smooth and shining finish, which distinguishes it from other etchants such as tetramethyl ammonium hydroxide (TMAH).

Dry etching was invented in the 1970's to solve the lack of a satisfactory silicon nitride etchant, particularly when aluminum lines were exposed [50]. Powered by external radio frequency energy, dry etching can be operated below 350 °C, even at room temperature in a plasma environment. One dry etching technique, the deep reactive ion etching technique, powered by inductively coupled high-density plasma, is capable of achieving a high aspect ratio up to 20:1 with a nearly 90 ° sidewall. This deep reactive ion etching process consists of a passivation cycle and an etching cycle. The use of the deep reactive ion etching technique has been reported in millimeter-wave components, e.g., a microstrip to rectangular waveguide transition [116]. Figure 6 depicts a micromachined waveguide structure using the deep reactive ion etching technique.

1.3 Enabling Technology: The Deep Reactive Ion Etching Technique

The mechanism of the deep reactive ion etching process is introduced in this section to provide a general guideline for the fabrication of the proposed passives in the following chapters. Figure 7 illustrates this process [41]. The deep reactive ion etching

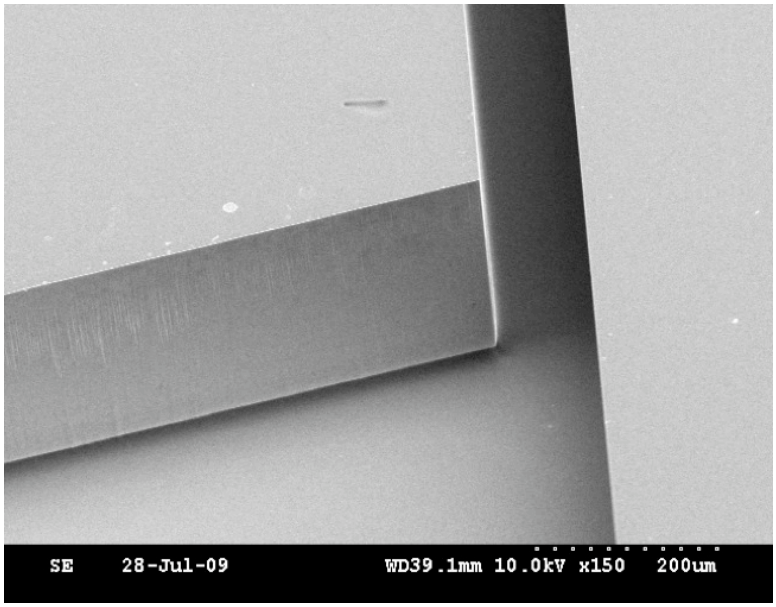


Figure 6: The SEM photo of a waveguide structure using the deep reactive ion etching technique at the Georgia Institute of Technology.

technique is a dry etching process that consists of two cycles: a passivation cycle and an etching cycle. In the passivation cycle, the plasma of C_4F_8 deposits a thin polymer layer on all surfaces. In the etching cycle, the gases of SF_6 and Ar are used. Accelerated by external radio frequency energy, the ion bombardment removes the polymer layer on the base much faster than that on the sidewalls. Once the silicon is exposed, the wafer is etched by fluorine species from the plasma of SF_6. The two cycles are alternatively repeated until a desired depth is reached.

In the following projects presented in this thesis, a straight sidewall close to 90° is expected. In reality, however, the profile of trenches is affected by many factors, including the pressure in an etching chamber, the flow rate of gases, the time for etching and passivation, the power of etching and passivation, and the exposed area of the silicon. Tuning these parameters in an inductively coupled plasma etcher to find a perfect recipe is a trial-and-error and time-consuming process. Therefore, understanding which knob to tune is crucial to achieving a nearly 90° sidewall. Figure 8 depicts the effects on sidewalls while the parameters of flow rates, time, pressure, and

power are being tuned [41].

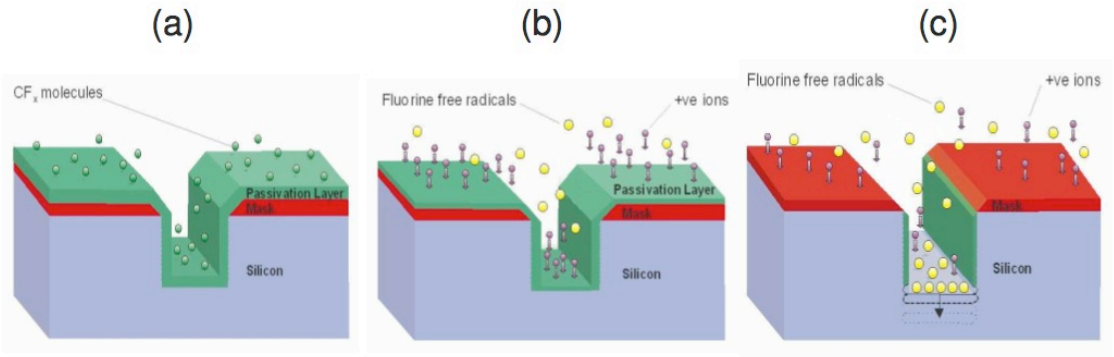


Figure 7: The deep reactive ion etching technique: (a) a thin polymer layer from C_4F_8 plasma is deposited on all surfaces; (b) the polymer layer is etched faster from the base than that from the sidewalls; (c) the exposed silicon is etched by fluorine species [41].

	U ± %	Etch Rate	Selectivity to mask	Profile ↑=re-entrant	Scalloping	Mask Undercut
SF6 Flow ↑	↔/↑	↔/↑	↔/↑	↑	↑	↑↑
C4F8 Flow ↑	↔/↓	↔/↓	↔/↑	↓	↓	↓↓
SF6 Time ↑	↔/↑	↔/↑	↔	↑	↑	↑↑
C4F8 Time ↑	↔/↓	↔/↓	↔	↓	↓	↓↓
Pressure ↑	↑↑	↑↑	↑	↑↑	↑	↑
Platen Power E & P ↑	↔	↑↑,↑	↓,↓	↑,↓	↔,↔	↔,↑
Coil Power E & P ↑	↔	↔/↔	↔/↔	↔/↔	↔/↔	↔/↔

Figure 8: The deep reactive ion etching trend [41]. The U denotes the uniformity; the E denotes the etching cycle; P denotes the passivation cycle. This figure gives the effect on uniformity, etch rate, selectivity to mask, profile, scalloping, and mask undercut while tuning the SF6 flow, C4F8 flow, SF6 time, C4F8 time, pressure, platen power, and coil power.

1.4 Process Flow

Figure 9 shows the process flow to fabricate millimeter and submillimeter-wave components using the deep reactive ion etching technique. First, a silicon wafer is rinsed to remove the organic residues. Then, a layer of silicon dioxide is deposited on both

sides of the wafer using the plasma-enhanced chemical vapor deposition process. After the deposition, a layer of photoresist is spun and patterned on top of the silicon dioxide layer. The exposed silicon dioxide layer is etched away using the dry-etching technique. After the photoresist residues are removed, the patterned silicon wafer is etched using the deep reactive ion etching technique for the desired depth. Then, the silicon wafer is flipped over, and the process is repeated starting from the spinning of the photoresist. Finally, the micromachined samples are released after removing the silicon dioxide layer. A thick metal layer of Ti/Cu/Au is deposited to form the metalized surfaces of waveguide structures. According to Equation 1, the skin depth is inversely proportional to the square root of operating frequencies. At 60 GHz, the skin depth of copper is about 0.2 μm. Therefore, a 1-μm thick metal layer behaves electrically as well as a solid conduct wall. The skin depth, δ_s, is given in the following equation:

$$\delta_s = \sqrt{\frac{2}{\omega \mu_0 \mu_r \sigma}} \tag{1}$$

where σ is the bulk conductivity in Simen/meter, μ_0 is the permeability constant $= 4\pi * 10^{-7}$ Henry/meter, and μ_r is the relative permeability.

1.5 Advantages of the Deep Reactive Ion Etching Method

In this research, a wide range of millimeter and submillimeter-wave components have been designed, fabricated, and characterized. Compared to other 3-D micromachining techniques, the deep reactive ion etching technique is suitable for mass production because it is a low-cost, parallel process. The process flow is CMOS compatible regardless of the crystal orientation of silicon wafers. In particular, the mechanical and chemical properties of silicon wafers have been extensively studied. In addition, no dielectric filling eliminates dielectric loss, which is the dominant loss at the high-frequency end. Therefore, the deep reactive ion etching technique is feasible

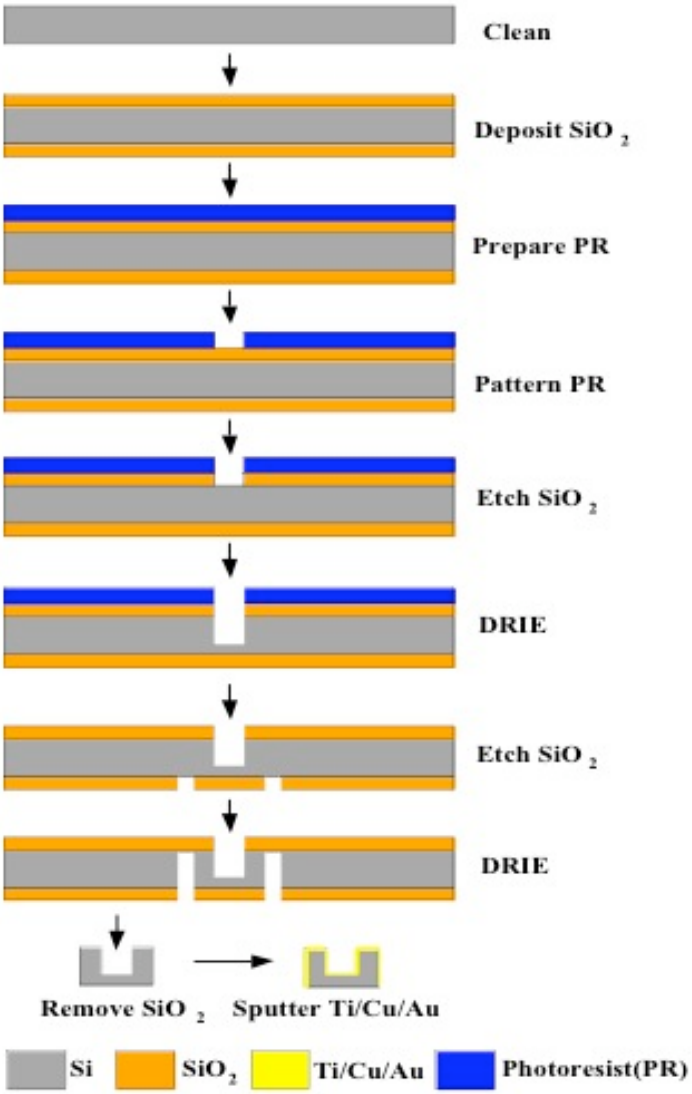


Figure 9: Fabrication flow of using the deep reactive ion etching technique. A waveguide passive is made with the use of split-block method by cutting along the E-plane center or H-plane center. Each half is fabricated using this fabrication flow. Then the fabricated two halves are put together to form the waveguide passive.

for providing high-precision and high-performance millimeter and submillimeter-wave components.

1.6 Contribution and Organization

In this work, the electrical performance of millimeter and submillimeter-wave components is investigated in the frequency band spanning from 60 GHz to 900 GHz. Chapter 2 investigates micromachined straight and meander waveguides from 75 GHz to 110 GHz using the deep reactive ion etching technique and analyze the tolerances of a micromachined straight waveguide. The results show that the straight waveguide has a measured insertion loss of 0.23 dB/cm−0.42 dB/cm from 85 GHz to 105 GHz. The meander waveguide has the measured insertion loss of 0.41 dB/cm−0.69 dB/cm from 90 GHz to 110 GHz.

Then, chapter 3 introduces a micromachined W-band bandpass filter. The three-pole Chebyscheff bandpass filter has 0.5-dB ripples in the passband and at least 30 dB attenuation at 9 GHz away from the center frequency. The measured center frequency is at 92.45 GHz. The passband insertion loss is between 1.1 dB and 1.3 dB with a bandwidth of 4.83 %. The measured responses demonstrate the feasibility of using the silicon micromachining technique to fabricate low-loss millimeter-wave passives.

Chapter 4 presents a W-band hybrid coupler and a W-band power divider. In this project, the hybrid coupler and the power divider are designed in the H-plane of a rectangular waveguide. The hybrid coupler uses a ridged waveguide 90° phase shifter to reduce phase deviation and a joint waveguide to achieve a broad bandwidth. The power divider utilizes a T-shaped topology. The simulated and measured responses show good agreement. Measured combining efficiency is reported by cascading the power divider and hybrid coupler.

Chapter 5 shows a novel micromachined wideband transition from a coplanar waveguide (CPW) to a rectangular waveguide from 75 GHz to 110 GHz. The transition is suitable for integration with planar circuits. The measured insertion loss of a back-to-back structure is 2.25 dB, and the measured return loss is better than 11 dB over the entire W-band. This transition is comprehensively analyzed and reported.

Chapter 6 introduces a waveguide filter that takes full advantage of the above transition. In the proposed filter, metal-coated probes are used to couple signals from CPW lines to cavity-based resonators. Therefore, the waveguide-based input and output ports are no longer needed. This design significantly reduces the size of the proposed filter. A measured response has a center frequency of 96.6 GHz, a bandwidth of 2.9%, and a passband insertion loss of 4.14 dB.

Chapter 7 presents high-Q tunable cavity resonators using planar tuning components. This project tackles the problem of using planar components to tune the resonance of a 3-D cavity resonator. This tunable cavity resonator can be used in the design of reconfigurable cavity-based modules for wireless communication systems.

Chapter 8 presents a 900-GHz frequency tripler with micromachined waveguide structures. The input of this 900-GHz tripler, powered by a 300-GHz tripler, is pumped into an input waveguide. The signals are coupled to a suspended microstrip line that supports the propagation in a TEM mode using an E-plane probe. The high and low impedance sections in the microstrip line assist the impedance matching of diodes and isolate the third harmonic signals from the input waveguide. The generated third harmonic signals are coupled to an output waveguide through the second E-plane probe. The background of THz signal sources, the design methodology of frequency multipliers, the topology of balanced diodes, the optimization of the use of full-wave simulators, and the measurement of the 900-GHz tripler are presented in detail. Finally, chapter 9 concludes the thesis by listing the contributions of the research and the publications of this work to date.

CHAPTER II

A W-BAND STRAIGHT WAVEGUIDE AND A W-BAND MEANDER WAVEGUIDE

In this chapter, a W-band straight waveguide and a W-band meander waveguide are designed and characterized to define the electrical performance of silicon micromachined waveguides using the deep reactive ion etching technique [42]. The micromachined W-band straight waveguide is a fundamental block to build more complicate waveguide passives. The meander waveguide can be used in traveling wave tubes that provide amplified radio frequency signals using an external electron beam. A high-frequency traveling wave tube is benefited from the demonstration of this micromachined W-band meander waveguide.

2.1 Meander Waveguide

Figure 10 shows the physical layout of the meander waveguide, which is designed in the E-plane of a waveguide. The meander waveguide consists of three sections: transition, meander, and transition. The meander section is optimized to achieve the minimum insertion loss. Two transitions connect the W-band signals from input and output to the meander section. Figure 11 shows the meander section in detail. The meander section has a height of 2.54 mm. The input and output use standard WR-10 waveguide flange. In Figure 11 , B denotes the width of the meander section. L denotes the length of the straight waveguide between two turns, and P denotes the diameter of an E-plane bend that connects the two straight parts. P is selected to be $0.427\lambda_g$ for a compact size. After the full-wave simulation using Ansofts HFSS, L equals to $0.831\lambda_g$, and B equals to $0.118\lambda_g$, where λ_g is the guided wavelength at

the center frequency. λ_g is given in Equation 2 for a TE_{10} mode.

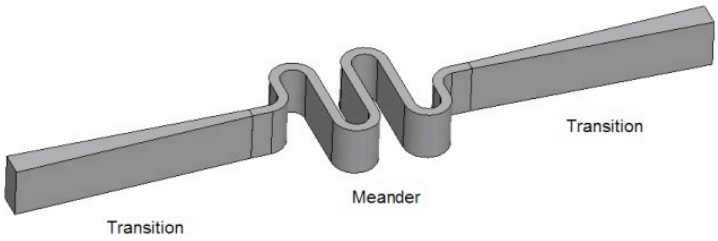


Figure 10: The physical layout of the meander waveguide. It consists of two transition sections and one meander section.

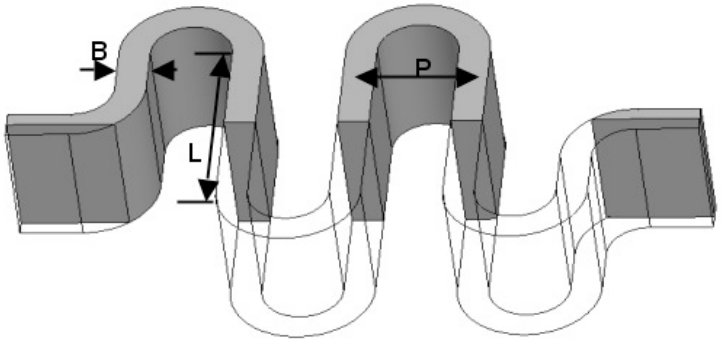


Figure 11: The meander section in detail.

$$\lambda_g = \frac{\lambda}{\sqrt{1 - (\frac{\lambda}{2a})^2}} \tag{2}$$

where a is the width of a rectangular waveguide and λ is the free space wavelength at the center frequency.

To optimize the transitions, a linear taper is chosen for its low insertion loss and easy fabrication. The electrical performance of the whole meander waveguide is simulated and reported in Figure 12. The dimensions are summarized in Table 1.

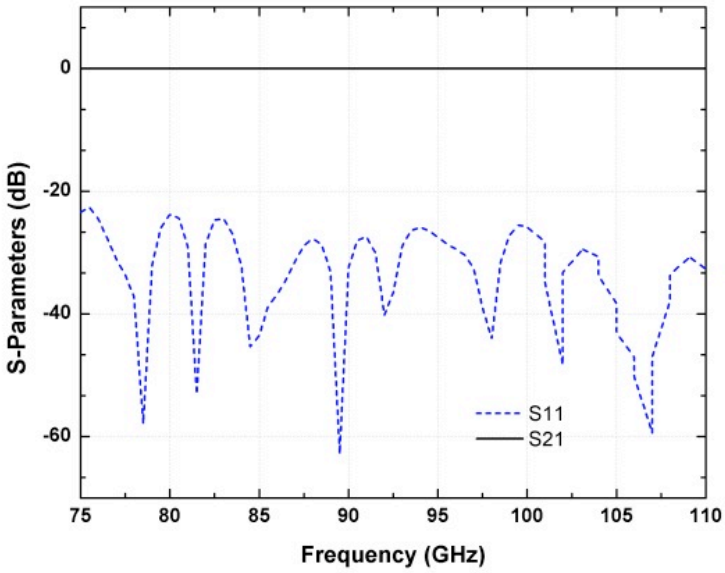


Figure 12: The optimization response of the meander section.

Table 1: Dimensions of the meander waveguide.

Dimensions	Value (mm)
P	1.8
L	3.5
B	0.5
Length of the transition	7.2

2.2 Straight Waveguide

A 1-inch long WR-10 straight waveguide is fabricated using the deep reactive ion etching technique. Figure 13 depicts a waveguide structure, which is cut in half along the center of the H-plane of a waveguide. Each half of the waveguide is etched individually and is assembled together to form the waveguide structure.

The two important tolerances in the deep reactive ion etching process are vertical striation and re-entrant angle. These two tolerances are drawn exaggeratedly in Figure 13 to show the details. The SEM photos of tolerances are shown in Figure 14. The re-entrant sidewall in a silicon trench comes from the lack of polymer if the time

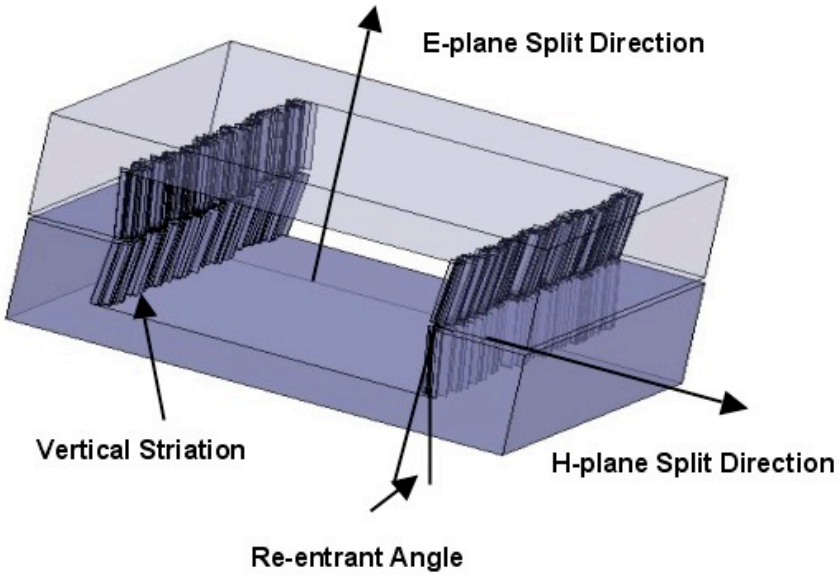
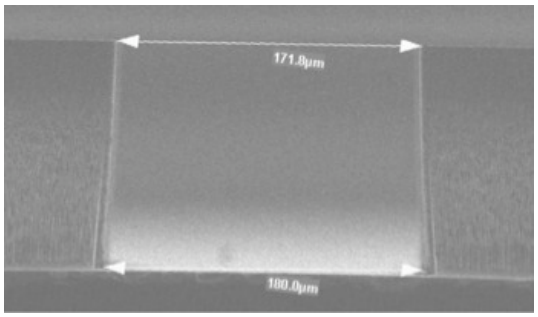
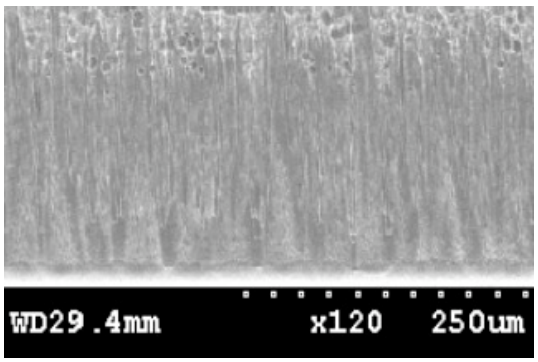


Figure 13: Tolerances in the fabrication using a H-plane split.



(a) Re-entrent angle.



(b) Vertical striation.

Figure 14: SEM photos of two physical characteristics important for practical waveguides.

of passivation cycle is not enough. Besides the time of passivation, several reasons can result in the re-entrant angle in the deep reactive ion etching, e.g. the power of etching or the time of etching. The bottom of the trench eventually becomes wider than the top of the trench in the etching process. In general, the re-entrant angle is less than a few degrees. The optimized recipe for a 90 ° sidewall depends on many variables: exposed size of silicon wafer, aspect ratio of etching, and desired depth of trench. The re-entrant sidewall in a H-Plane split topology is evaluated by simulation and shown in Figure 15. With the increase in the re-entrant angle, the cross section is no longer a standard WR-10 waveguide. The propagation mode of waveguides is usually dominated by a TE_{10} mode, unless higher modes are excited. The wave impedance is determined by Equation 3. The wave impedance is real when the propagation constant is real in a propagation mode. The wave impedance is imaginary when the propagation constant is imaginary in an evanescent mode. The deformation of the cross section due to the re-entrant angle decreases the wave impedance and result in an impedance mismatch with a WR-10 waveguide. Therefore, the re-entrent angle should be minimized to reduce the impedance mismatching. As predicted, the simulation shows that the increased re-entrant angle degrades the impedance matching and return loss.

$$Z_{TE} = \frac{k\eta}{\beta} \tag{3}$$

Where Z_{TE} is the wave impedance, k is the wave number, η is the intrinsic impedance of the material filling the waveguide, and β is the propagation constant that is affected by the dimensions of the waveguide structure.

Vertical striations on a sidewall are shown in Figure 13 and Figure 14. A heavy sidewall passivation may lead to a vertical striation [53]. To evaluate the impact on the electrical performance, a vertical striation sidewall is simulated using Ansofts HFSS. The height of each striation follows a uniform distribution. The mean value

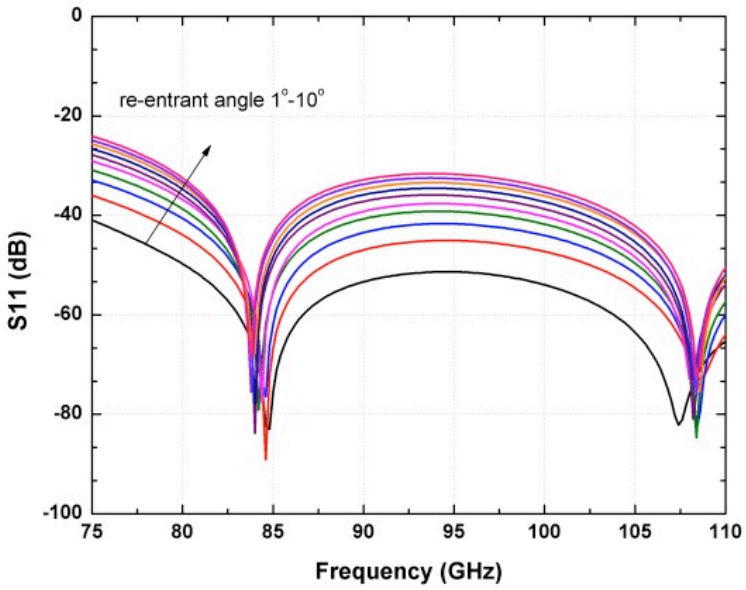


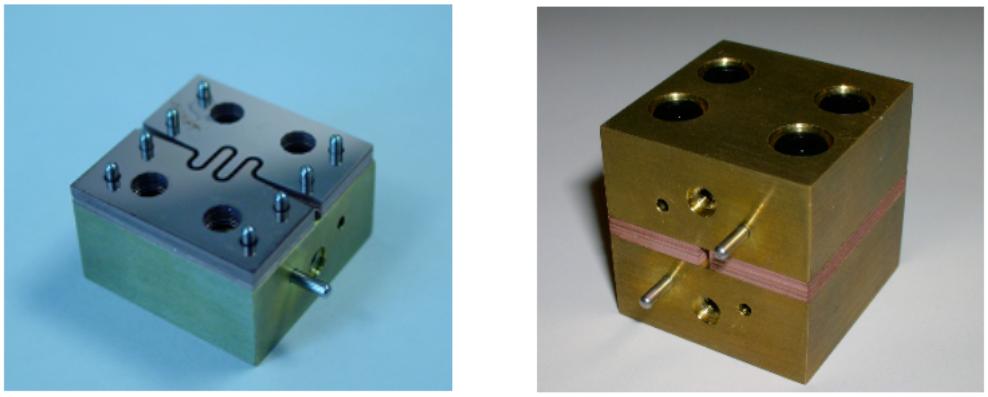
Figure 15: The simulation of re-entrant angle along a H-plane split.

and standard deviation are chosen according to the vertical striations in fabrication. The width of the virtical striation is less than 25 μm, and the roughness is less than 50 μm. The simulation shows that a return loss is better than 24 dB from 75 GHz to 110 GHz when the sidewall is well covered with 5-μm thick copper. The return loss is not affected much by the vertical striation because the deformation of the cross section is less than 50 μm and is relatively small compared with the 2.54 mm long broad side. The insertion loss, however, will increase because of the extended surface current path due to the vertical striation and the thin skin depth in the W-band.

2.3 Fabrication and Assembly

Four 525-μm and one 400-μm thick low resistivity (10−20 ohms-cm) silicon wafers were used in the fabrication process. Four layers of micromachined silicon samples are stacked together to form both the straight waveguide, the meander waveguide, and WR-10 waveguide flanges. The width of a WR-10 waveguide is 2.54 mm, and the height of it is 1.27 mm. The splits of the waveguide are on the E-plane, but

not along the center. The current path is cut if a small gap exists between two adjacent samples. This current discontinuity can result in a radiation loss, which will deteriorate the insertion loss. Alignment pins are used to align the stacked silicon samples together. Figure 16(a) shows the assembled meander waveguide in a fixture. Figure 16(b) shows the assembled fixture and the WR-10 waveguide flange. The 1-inch long fixture consists of two blocks: a bottom block with eight alignment pins and a top block. After the silicon samples are put on the bottom block, the top block is assembled. Four screws hold the top and bottom blocks together and remove the gaps between silicon samples. A UG-387 waveguide flange is formed with the metal fixture and micromachined silicon samples.



(a) Silicon Samples. (b) Fixture and Flange.

Figure 16: Silicon samples and assembled fixture.

2.4 Measurement and Conclusion

The meander waveguide and the straight waveguide are measured using Agilent Vector Network Analyzer 8510XF. The calibration is applied before the measurement using a Hewlett-Packard calibration kit W11644A. The measurement setup is shown in Figure 17. A measured insertion loss and a measured return loss of the straight waveguide are reported in Figure 18 and Figure 19. The S-parameters of the meander waveguide are shown in Figure 20 and Figure 21. The additional loss of the meander waveguide below 90 GHz may come from the alignment tolerance, the re-entrant

sidewall, and the undercut in the fabrication. The measured insertion loss of the straight waveguide is between 0.23-0.42 dB/cm over 85 GHz-105 GHz. The insertion loss of the meander waveguide is between 0.41-0.69 dB/cm over 90 GHz-110 GHz.

The measured results show great response compared with the existing waveguides published in the literature. In [43], the attenuation of a planar CPW line is about 1.5 dB/mm on a normal silicon wafer and about 0.5 dB/mm on a grooved silicon wafer. In [45], the microstrip line is characterized up to 90 GHz. The measured result has an insertion loss of 0.15 dB/mm at 90 GHz. The metal WR-10 waveguides reported by Aerowave have the loss of 2-1.4 dB/FT [44].

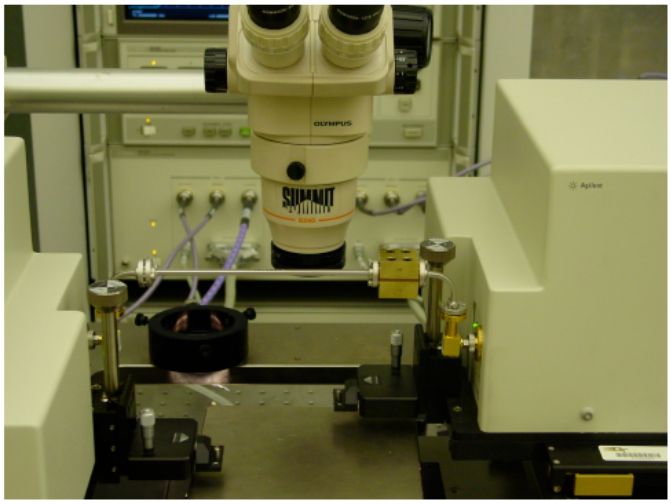


Figure 17: The measurement setup.

Figure 22 gives the comparison of this work with the existing W-band 3-D micromachined waveguides and planar waveguides that are on low-loss substrates, e.g. liquid crystal polymer, GaAs, and polyimide. The comparison shows the micromachined waveguides using the deep reactive ion etching technique have the competing performance compared with other 3-D micromachined waveguides and much less attenuation loss compared to the planar passives.

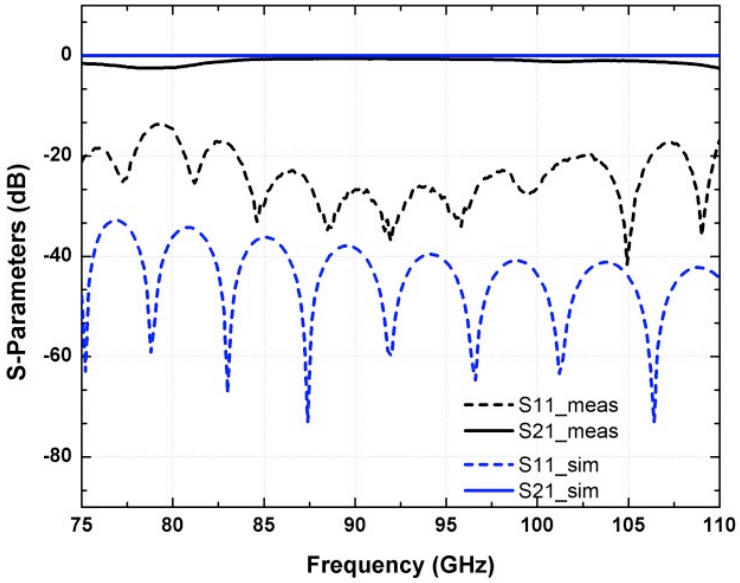


Figure 18: The measurement and simulation of the straight waveguide.

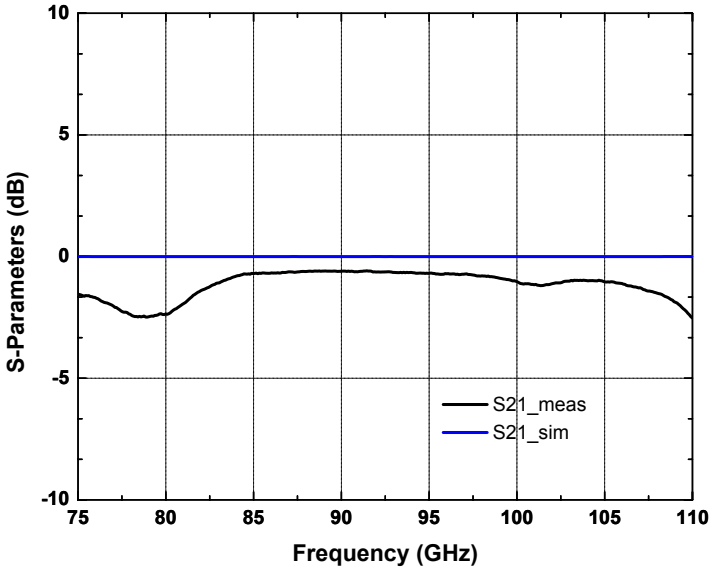


Figure 19: The measured and simulated S21 of the straight waveguide.

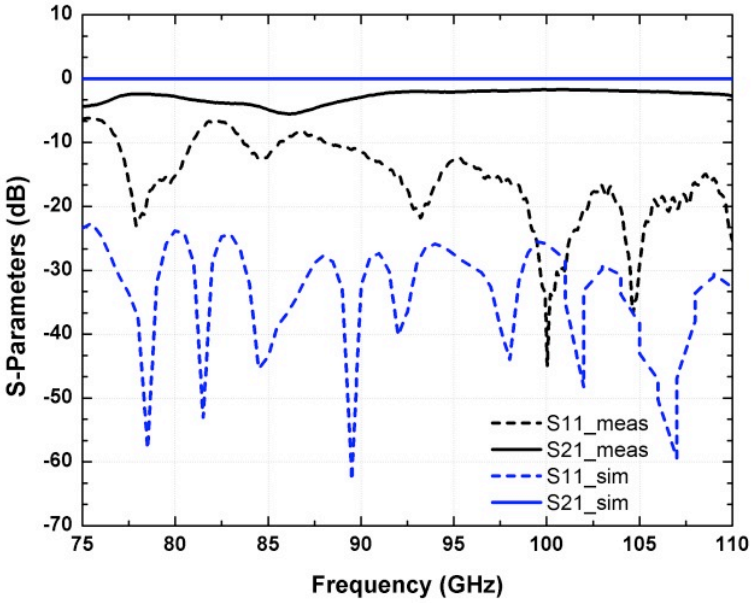


Figure 20: The measurement and simulation of the meander waveguide.

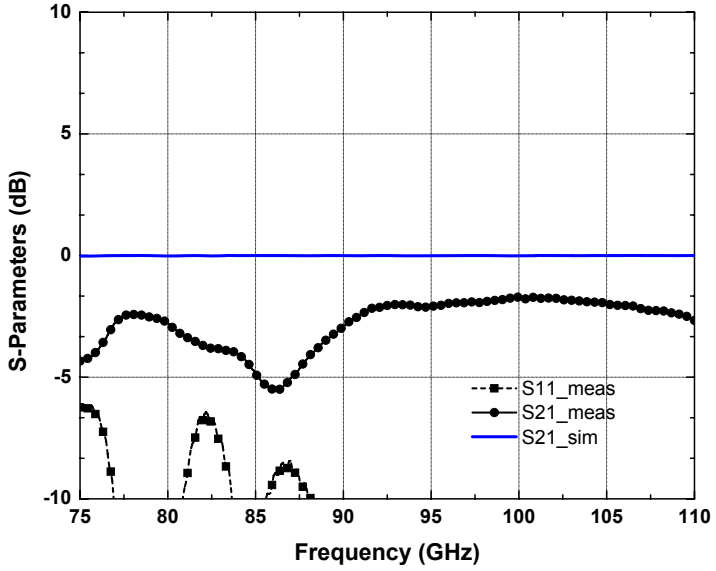


Figure 21: The measured and simulated S21 of the meander waveguide.

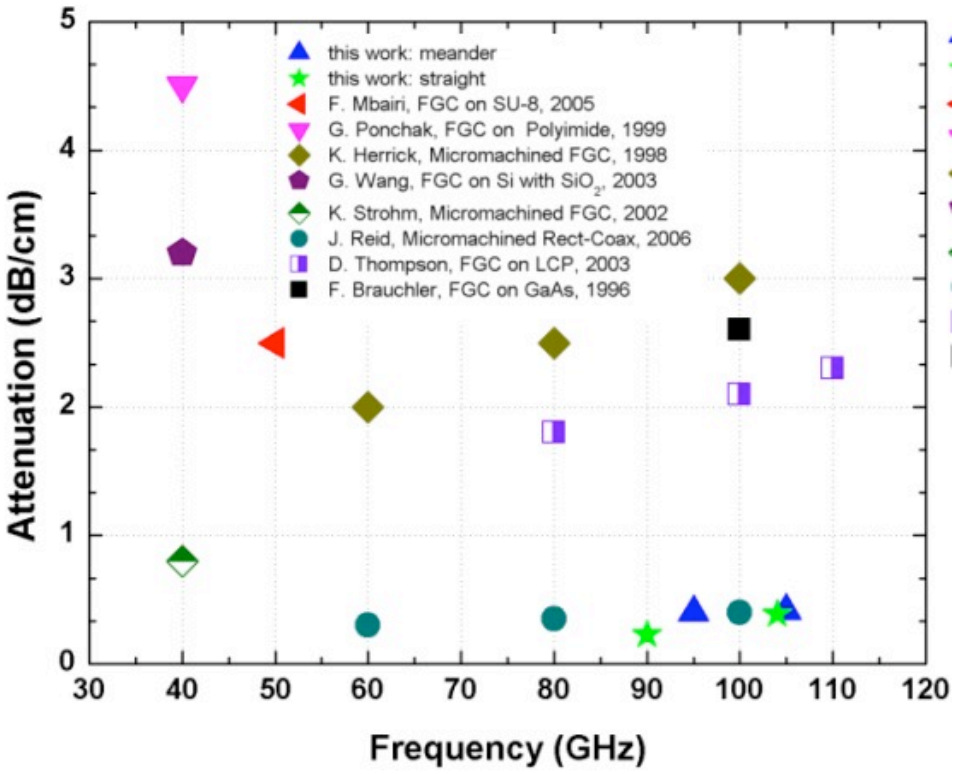


Figure 22: A comparison of this work with existing works, including micromachined finite-ground-coplanar (FGC) lines and micromachined rect-coax waveguides.

CHAPTER III

A W-BAND THREE-POLE BANDPASS WAVEGUIDE FILTER

3.1 Design Topology

A three-pole waveguide filter is presented with the theoretical background in [47]. The rectangular waveguide filter has four pairs of irises, shown in Figure 23. The WR-10 rectangular waveguide flanges are used to guide the signals in and out. The waveguide filter is designed using three cavities that are inductively coupled to each other. The simulated responses have a center frequency of 94.2 GHz and a bandwidth of 3.5%. The passband of the filter has 0.5-dB Chebyscheff ripples and has at least 30-dB attenuation at 9 GHz away from the center frequency. The W-band filters have been exploited in the literature. In [10], a micromachined W-band filter using a shield membrane microstrip resonator is reported with a passband insertion loss of 3.6dB and a bandwidth of 6.1%. In [59], a W-band bandpass filter with a bandwidth of 5.6% is designed without providing the measurement results.

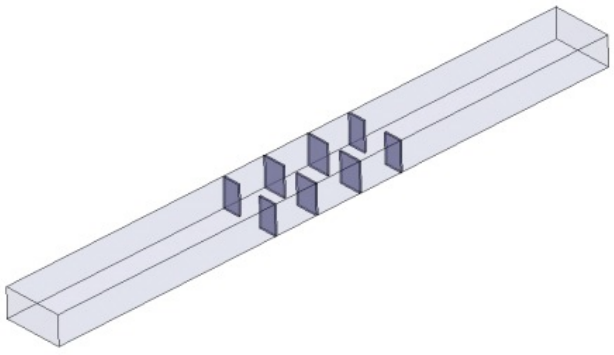


Figure 23: The physical layout of the waveguide filter.

3.2 Simulation

The guided wavelengths are calculated at the center frequency. The normalized prototype frequencies are determined, and the attenuation is predicted. Then, the dimensions of coupling irises and the space between these coupling irises are obtained using the equations in [48] [49]. Finally, the filter is optimized using a full-wave simulator, Ansoft's HFSS 9.2. A copper layer is used to cover all of the internal surfaces of the waveguide structure. The input and output are inductively coupled to the first and the third resonators. These two resonators are coupled to the resonator in the middle respectively. The optimized S-parameters are reported in Figure 24.

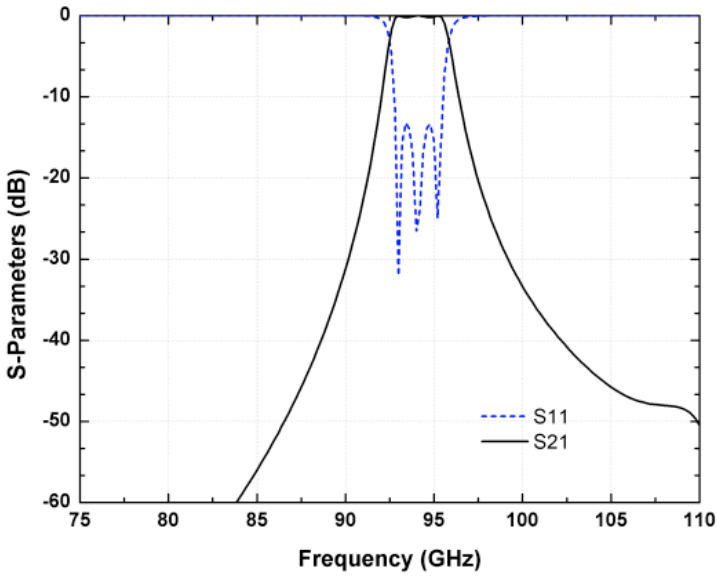


Figure 24: The simulated response of the three-pole filter.

3.3 Fabrication and Measurement

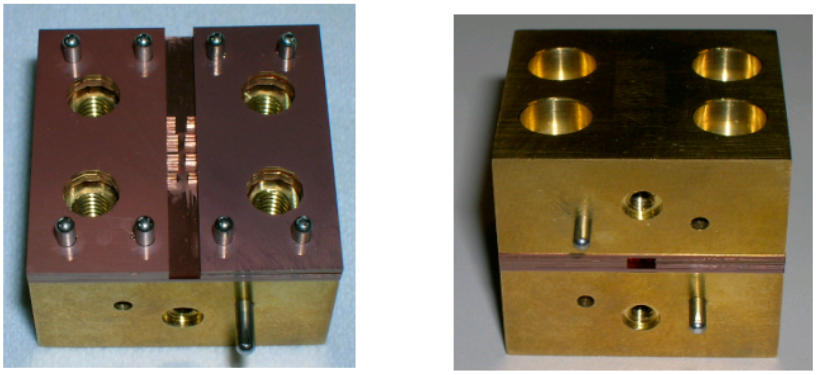
Four 525-μm thick silicon layers were used and were denoted as S1, S2, S3, and S4 from top to bottom. The S1 and S4 were etched on top for a depth of 110 μm and were released from back with a different pattern. The S2 and S3 were etched from both sides with the same pattern. The first step of the preparation was a wafer cleaning

process. Then, a silicon dioxide layer with a thickness of 3.3 μm was deposited on top of the wafer using Uniaxis PECVD. After the silicon dioxide deposition, photoresist was spun on top of it. The exposed silicon oxide layer was etched using dry etching. Finally, the photoresist residue was removed and the silicon was etched using STS ICP with the deep reactive ion etching process for a depth of 110 μm. The silicon substrate was flipped after the dry etching and was released from the back. The metallization was applied on both sides of the silicon samples with Ti and Cu for a total thickness of 5 μm.

A re-entrant angle is observed in the deep reactive ion etching processing. In our process, the re-entrant angle is usually less than four degrees. However, for a 525-μm thick wafer, a 4 degree re-entrant angle equals to a 36.7-μm difference when the wafer is etched through. In our design, the width of an irises is 75 μm. Etching through the entire wafer will leave the bottom of an iris no more than 3 μm and lead to fragility in the assembly. To solve this problem, a backside alignment and a double-side etching are used to reduce the effect of re-entrant angle.

A fixture, shown in Figure 25, is designed and fabricated to facilitate the measurement. The 1-inch long fixture consists of two blocks. The height of each block is 0.458 inch. On the bottom block, eight alignment pins are used to align the stacked silicon samples and the top block. Four screws are used to hold the stacked silicon samples and the bottom block. The WR-10 flanges are enabled in the front and at the back of the fixture. The fixture and the stacked silicon samples are shown in Figure 25.

The measurement of the waveguide filter was taken using Agilent Vector Network Analyzer 8510 XF. The measurement setup was the same as that in Chapter 2. The calibration was applied with HP W11644A calibration kit. The measured data are shown in Table 2. The insertion loss and the return loss of the waveguide filter are reported in Figure 26. The insertion loss in the passband is only 1.1 dB$-$1.3 dB. The



(a) The silicon samples with the fixture.

(b) The fixture and the flange.

Figure 25: The silicon sampls and fixture. In (a), the silicon samples are assembled and aligned through the alignment pins in the fixture. In (b), the fixture and the silicon samples are ready for the measurement. A UG-387 flange forms at the input port and output port.

measured center frequency is at 92.45 GHz. The measured bandwidth if 4.83%. The measured attenuation is more than 34 dB at 9 GHz away from the center frequency.

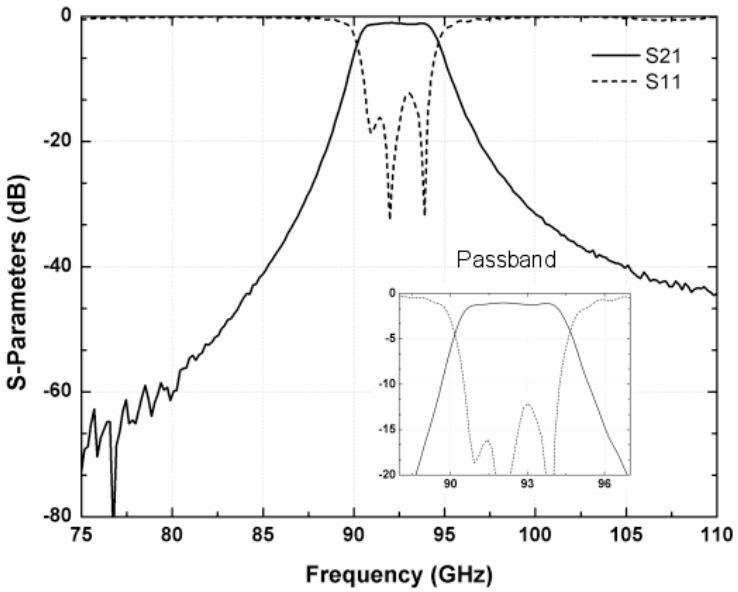


Figure 26: The measured insertion loss and return loss.

Table 2: The measured data of the W-band filter.

Measured parameters of the filter	Measured value
Center frequency	92.45 GHz
Bandwidth	4.83%
Insertion loss	1.1 dB to 1.3 dB
Attenuation 9 GHz away from center frequency	>34 dB

3.4 Conclusion

The shifted center frequency and the wider bandwidth, compared with Figure 24, come from the position tolerance of the alignment pins. Although the tolerance of photolithography and micromachining technique is on the level of 1 μm, the tolerance of the alignment pins from machine shop is on the level of mil (1 mil = 25.4 μm). The alignment pins are put slightly towards the edges. This tolerance leads to a wider cavity and a wider opening between two irises. The wider cavity results in a shifted center frequency toward low frequency end. The wider opening increases the coupling between two adjacent resonators. The increased coupling separates the resonances and leads to a wider bandwidth. Simulations of the tolerance are shown in Figure 27. The measured results have great agreement with the simulations using a 30-μm tolerance. Figure 28 depicts the comparison of this work with other existing micromachined filters in terms of the passband insertion loss and the center frequency.

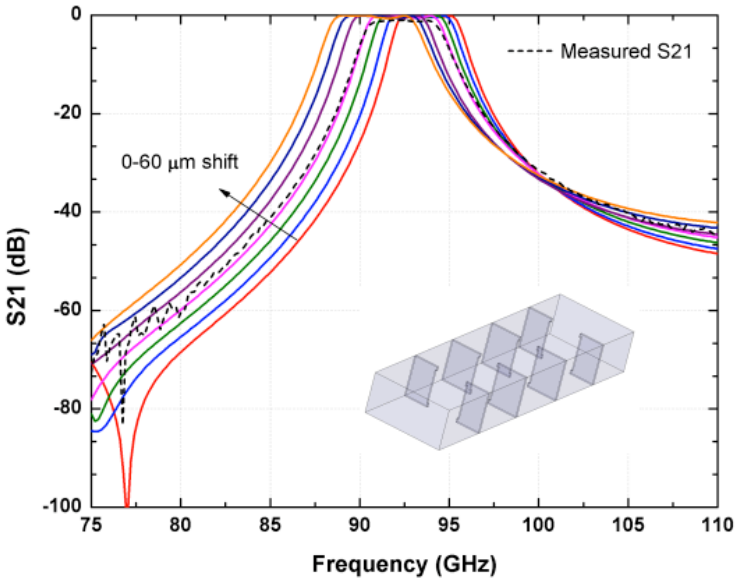


Figure 27: The simulations of the W-band filter by sweeping the shift of silicon samples toward the edges from 0-60 μm with a step of 10 μm. The shift results in a wider opening between adjacent resonators and a larger volume of each resonator.

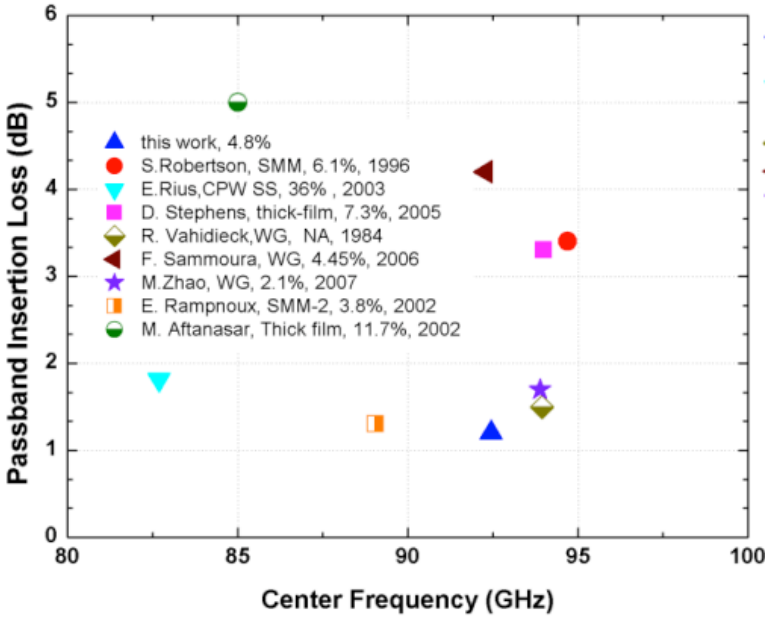


Figure 28: Comparison of this work with other existing micromachined filters.

CHAPTER IV

A W-BAND HYBRID COUPLER AND A W-BAND POWER DIVIDER

In this chapter, a silicon micromachined W-band hybrid coupler and a power divider using the deep reactive ion etching technique are presented. They are designed in the H-plane of a rectangular waveguide. The hybrid coupler has a ridged waveguide 90 ° phase shifter and a joint waveguide. The power divider utilizes a T-shaped configuration. The simulated response and measured response presented in this chapter show good agreement. Then, the measured combining efficiency is measured after cascading the power divider and the hybrid coupler.

Several waveguide couplers and power dividers have been investigated in the literature. In [50], a waveguide-based H-plane hybrid coupler centered at 11.424 GHz with 500 MHz bandwidth is reported. In [51], a 10-60-GHz directional coupler is presented using shielded membrane microstrip lines. In this chapter, the proposed W-band hybrid coupler and the power divider are presented with 31.6-GHz and 27.12-GHz frequency range, respectively, when the return loss is greater than 10 dB. The waveguide circuits presented here can be easily integrated with the transition in [52] to build a wafer-scale W-band millimeter wave front-end.

4.1 Design of the Hybrid Coupler

The hybrid coupler, shown in Figure 29, has four ports: Port 1 (input), Port 2 (through), Port 3 (coupled), and Port 4 (isolated). The four ports are connected to the joint waveguide through H-plane bends respectively, except that Port 1 is connected to a ridged waveguide 90 ° phase shifter first. The resonant frequency f_{301}

is accommodated by the joint waveguide and is defined by d and g in Figure 29. The Equation 4 gives the resonant frequency.

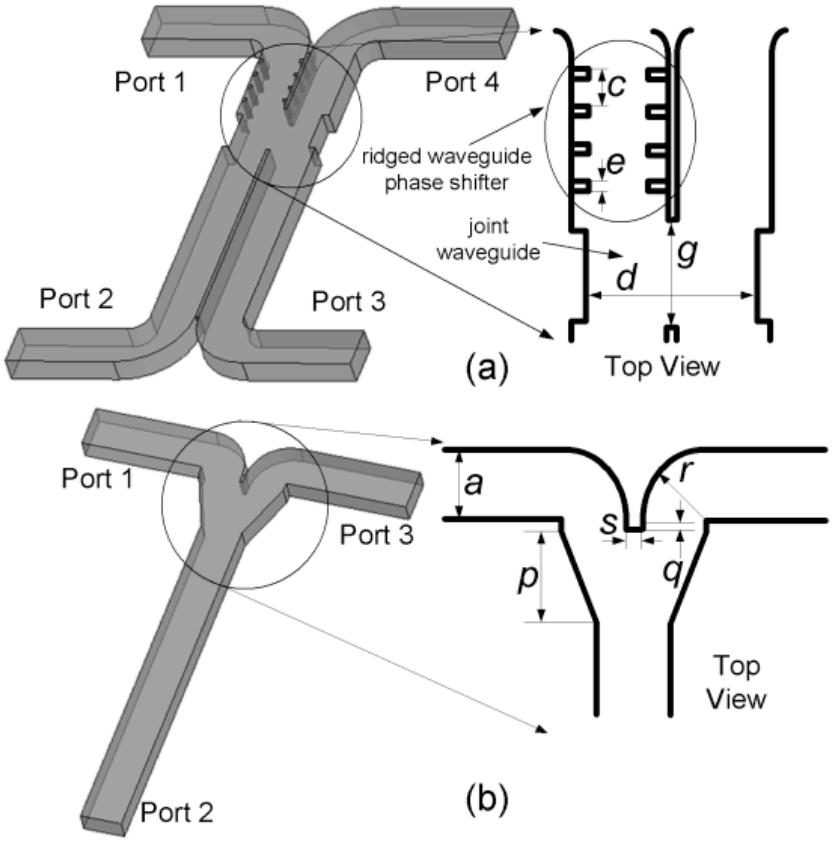


Figure 29: The topology of (a) the hybrid coupler and (b) the power divider.

$$f_{mnp} = \frac{c_0}{2\pi}\sqrt{(\frac{m\pi}{d})^2 + (\frac{n\pi}{b})^2 + (\frac{p\pi}{g})^2} \tag{4}$$

where d, b, and g are the width, height ,and length of the joint waveguide, and c_0 is the speed of light. The width d is reduced to less than twice of the WR-10 waveguide width for shifting f_{301} to higher frequency and achieving a broad bandwidth. The impact of d is investigated to show the return loss versus frequency in Figure 30. With an increase of d, the return loss is improved at the low-frequency end, but is worsened at the high-frequency end. A ridged waveguide 90° phase shifter using inductive irises is designed instead of using a quarter wavelength waveguide. The iris

spacing is given in [53].

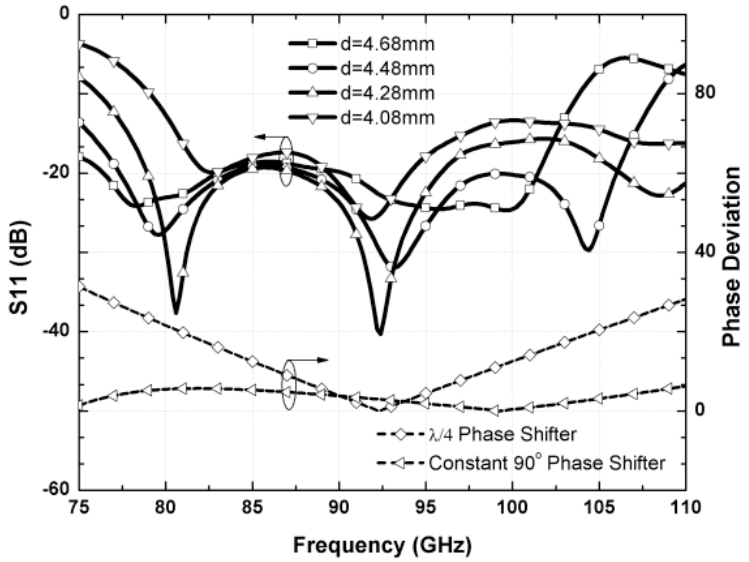


Figure 30: Simulated return loss vs. frequency with different d as well as the phase deviations of ridged waveguide 90 ° phase shifter and a quarter waveguide phase shifter.

4.2 Design of Power Divider

The T-shaped power divider, shown in Figure 31 , can split the signals from Port 2 and obtain two same phase signals at Port 1 and Port 3. The equivalent circuit of the H-plane waveguide bend includes a shunt inductor with susceptance that is a function of r [54]. The thickness of the iris is optimized and reported in Figure 31. As can be seen, the return loss is improved with the decreasing of iris thickness. The 200-μm thick iris is chosen to facilitate the fabrication. The waveguide circuits are split along the center of the H-plane. Each circuit is formed by two 1-mm thick silicon samples. The WR-10 waveguide flange is enabled by two silicon samples and the metal fixture.

The silicon dioxide was deposited on a pre-cleaned double-side polished 1-mm thick wafer using Unaxis PECVD. A photoresist (PR) mask was used to pattern the silicon dioxide using plasma thermal ICP. After the removal of residues, the wafer was

etched using STS ICP with a depth of 635 μm. Then, the silicon wafer was flipped and etched from the backside to release the sample. A layer of Ti/Cu/Au is sputtered on the silicon samples. The two silicon samples of the coupler are shown in Figure 32. Figure 32 also shows the WR-10 waveguide flange formed by the fixture and silicon samples.

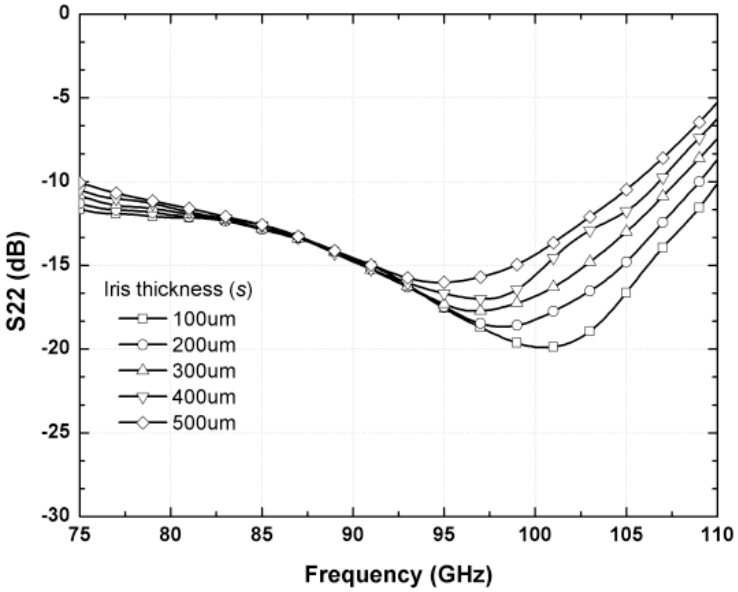


Figure 31: Simulated return loss against frequency with different iris thickness.

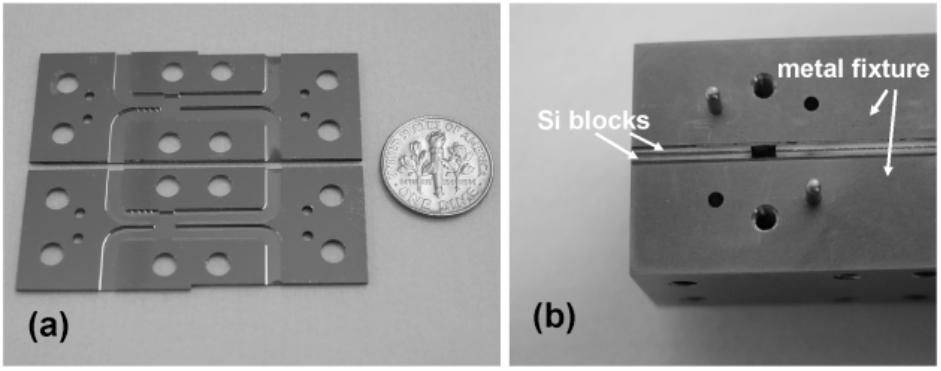


Figure 32: (a) Silicon blocks of the coupler; (b) WR-10 waveguide flange.

4.3 Measurement and Conclusion

The measurements are taken using Agilent 8510 XF VNA. In Figure 33 , the measured isolation and return loss of the hybrid coupler are greater than 17 dB over 75 to 105 GHz. The average coupling of the hybrid coupler is 3.4 ± 0.4 dB over 85 to 100 GHz.

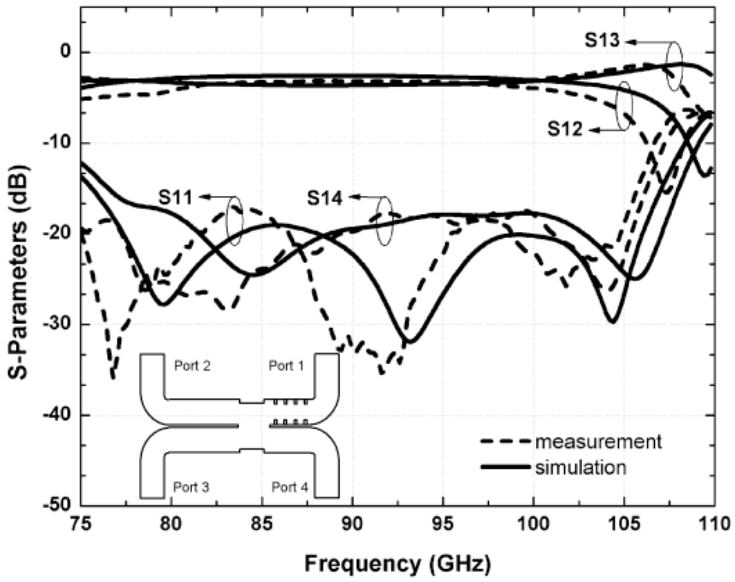


Figure 33: The S-parameters of the hybrid coupler.

In Figure 34 , the loss of the power divider is 0.6 ± 0.6 dB from Port 2 to Port 1 over 75 to 105 GHz; the return loss is greater than 10 dB over 27.12 GHz [47]. The dip in the measured S21 at 107 GHz is shifted from the dip out of the W-band at 114 GHz. The frequency shift is caused by the assembly and fabrication tolerances. The hybrid coupler and the power divider are cascaded to measure the combining efficiency at Port 3 of the hybrid coupler, shown in Figure 35. An Agilent signal generator 8362B and an Agilent source module 83558A are used to generate W-band signals that are fed into Port 2 of the power divider. The split signals are fed into Port 1 and Port 4 of the hybrid coupler. An Agilent power sensor W8486A and power meter E4419B are used to measure the power at Port 3 of the hybrid coupler. The efficiency is reported in Figure 35 after calibrating out the loss of the power divider

and the metal waveguide bends. The measured combining efficiency is greater than 80% between 85 GHz and 105 GHz. The low combining efficiency above 105 GHz comes from the dip in Figure 34 at 107 GHz. The dip in Figure 34 at 107 GHz comes from the dip at 114 GHz, which is out of the interested frequency band. The tolerances in the fabrication and assembly lead to the frequency shift to the lower frequency end.

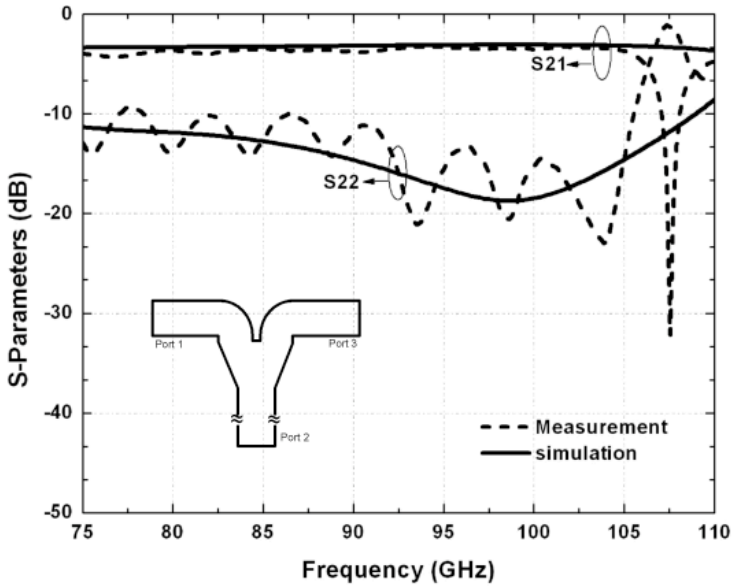


Figure 34: The S-parameters of the power divider.

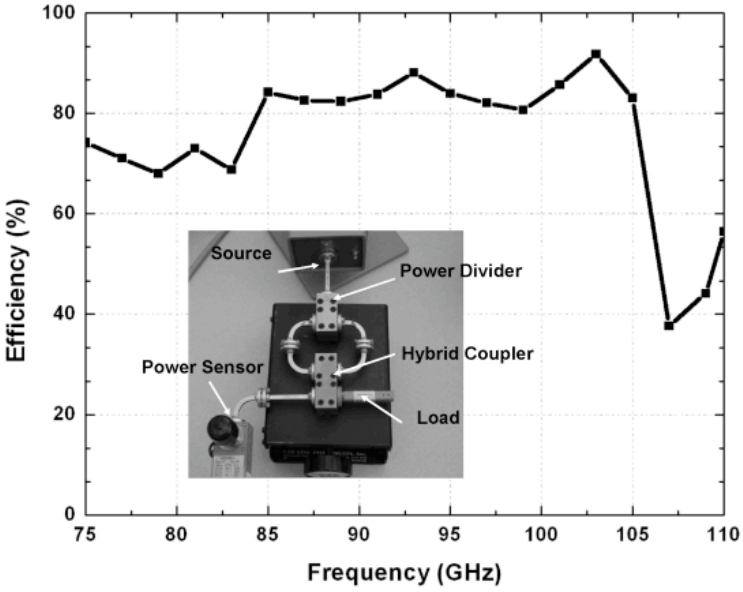


Figure 35: The measured combining efficiency after cascading the power divider and hybrid structure.

CHAPTER V

A WIDEBAND COPLANAR WAVEGUIDE TO RECTANGULAR WAVEGUIDE TRANSITION

Communication and satellite systems are seeking a fully integrated solution where waveguide components can be accessed through planar circuit board circuits such as printed microstrip and coplanar waveguide lines. Some intrinsic obstacles in this integration effort can be tackled through reconciling many fundamental differences that exist between planar and waveguide transmission lines. A rectangular waveguide has the advantages of low loss and high power capacity. The traditional rectangular waveguide at low frequencies , however, is bulky and is not suitable for the system-on-chip integration. Nevertheless, the size of rectangular waveguides shrinks dramatically in the millimeter-wave and submillimeter-wave frequency ranges [55]. Meanwhile, the loss of other compact planar transmission lines, such as microstrips, keeps increasing when the operating frequency goes up. The integration of sub-systems into a packaged solution with a combination of planar and waveguide components provides advantages in terms of high performance and reduced size. For this reason, it is crucial to building an understanding of planar-to-waveguide transition structures and their application in microwave component designs at millimeter-wave frequencies.

5.1 Existing CPW-to-Waveguide Transitions

In the existing approaches, transitions [55] [56] [57] with conventional machining techniques are not easily adopted by the micromachining, which is feasible for the integration of submillimeter-wave circuits, shown in Figure 36. The transitions from planar waveguides to substrate-integrated rectangular waveguides are reported [59]

[60] [61] [62]. These transitions have the advantages of using a low-cost print circuit board process. However, the substrate-integrated rectangular waveguides suffer reduced Q-factor due to the dielectric filling as well as the relatively large minimum slot and linewidth. In the meantime, several transitions are demonstrated using the low temperature co-fired ceramic (LTCC) technique not only from the planar waveguide to the rectangular waveguide [63] [64], but also from the laminated waveguide to the air-filled waveguide [65]. These transitions using the LTCC technique provide good responses, although they are limited by a via fence to form a cavity. The transitions from a CPW line to a rectangular waveguide on a silicon substrate are reported using either wet etching or dry etching techniques in [66] [67]. The coupling probe is fabricated separately and is assembled on the substrate.

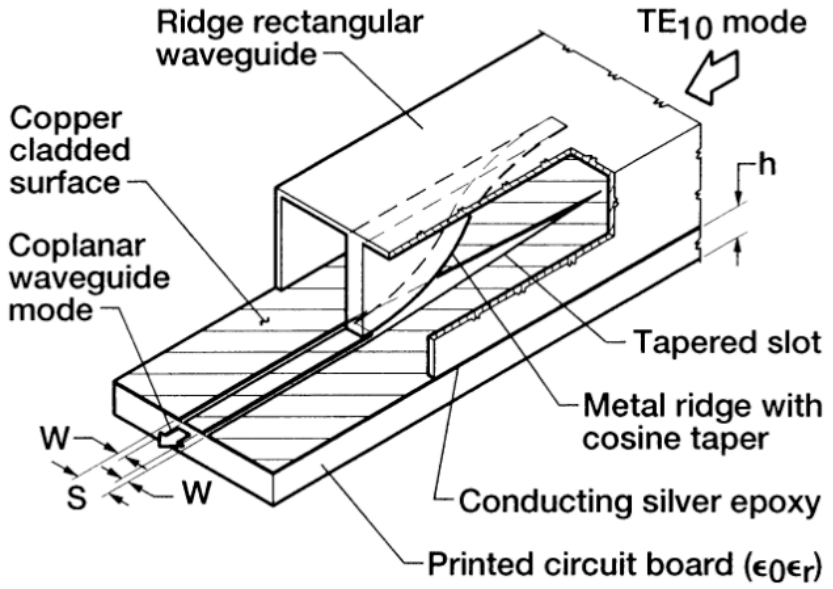


Figure 36: An existing wideband CPW-to-waveguide transition [58].

5.2 The Proposed Transition

In this section, a novel transition is proposed. It has the advantage of high precision and friendly mass production using silicon micromachining and thick film surface micromachining techniques. The CPW, probes, and rectangular waveguides are integrated on the same side of a substrate. The measured S-parameters of the back-to-back structure are quite encouraging. The comprehensive design analysis of the transition is given as well as the parameters study. The fabrication, experimental results, and the discussion are finally presented. This CPW to rectangular waveguide transition, shown in Figure 37 and Figure 38, consists of two sections: a section from a CPW line to a coaxial structure and a section from the coaxial structure to a rectangular waveguide. The CPW line to the coaxial structure transformation is simple to implement since they both support TEM (or quasi-TEM) mode propagation; the characteristic impedance matching geometry can be realized. The excitation of the dominant TE_{10} mode of a rectangular waveguide using a coaxial structure has been well established. The outer conductor of coaxial structure is on the broad wall of rectangular waveguide, while the probe as the inner conductor extending into the rectangular waveguide through an aperture. This section can be optimized through adjusting the height of probe in the rectangular waveguide and the length of backshort, which is the distance from probe to the waveguide short. The impedance presented to the extending probe by the rectangular waveguide is the characteristic impedance of the waveguide shunted to the impedance introduced by a backshort. Equation (5) calculates the input resistance R_0 presented to the coaxial structure [68]:

$$R_0 = \frac{Z_w}{2abk_0^2}(1 - e^{-2j\beta l_p})^2 \tan^2 \frac{k_0 H}{2} \tag{5}$$

Where, Z_w is the wave impedance of the waveguide in a TE_{10} mode, a and b are the dimensions of the waveguide, k_0 is the wave number, β is the propagation constant, l_p is the length of the backshort and H is the height of the probe in the

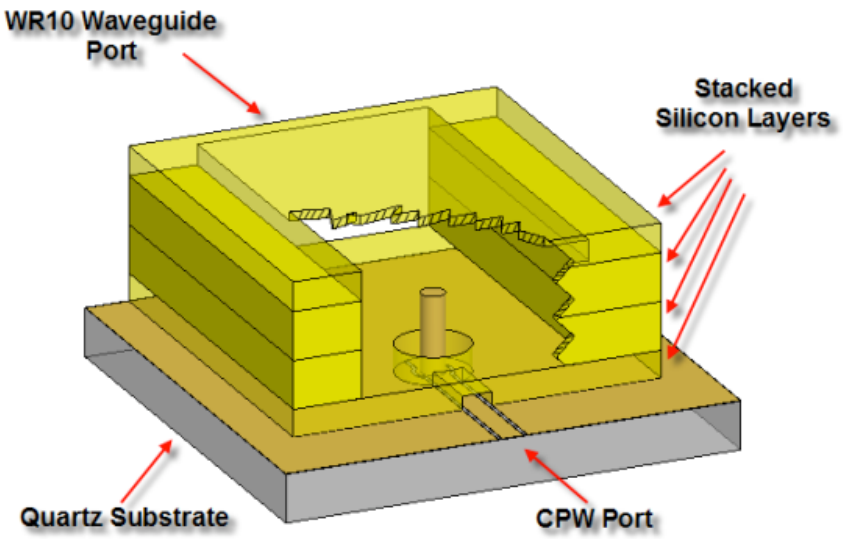


Figure 37: The schematic diagram of the transition.

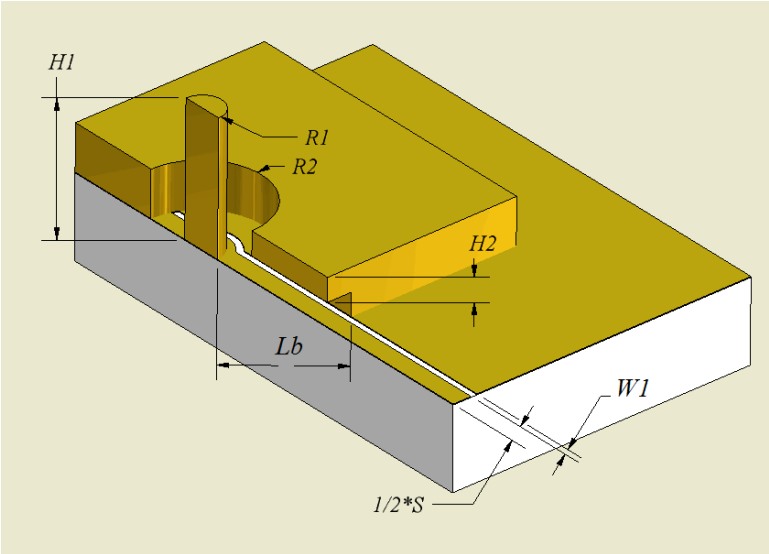


Figure 38: The CPW and the coupling probe (The transition is cut in half along the center of the broad wall due to its symmetry, and the metalized silicon sidewalls with thickness of T are not shown).

rectangular waveguide. In Figure 38, the length of backshort is $L_b + R_1$. $H1$ denotes the total height of the probe including two parts: the height of probe in the rectangular waveguide (H) and the height of probe in coaxial structure that is 300 μm in this design. H_2 represents the remaining thickness of the wafer after a tunnel is etched to

accommodate the CPW feeding. R_1 is the radius of the probe. S is the width of the inner conductor of the CPW line. W_1 is the width of the CPW slots.

5.3 Optimization of the Transition

The initial values of H and the length of the backshort can be determined through matching the impedance from the coaxial structure to the rectangular waveguide. This design rule initially gives the height of the probe in rectangular waveguide over half of the waveguide height. This configuration is hard to implement due to the aspect-ratio limit in fabrication. The height of a standard WR-10 waveguide is 1.27 mm and half of it is over 600 μm. The total height of the probe, H_1, will be close to 1 mm, including the coaxial part. To get a sufficiently good impedance matching while using a relatively short probe, the aperture radius on the broad wall is used as an additional design variable. Decreasing the probe height in rectangular waveguide is equivalent to reducing the coupling between the probe and the waveguide. Different from the current probe transition in [62], an impedance transformation is taken into account [69]. This open-circuited probe transition is suitable for wideband design [70].

To compensate for the mismatching over wide bandwidth, a short-end CPW stub is introduced, which improves the transition and provides another tuning variable in the whole transition. Meanwhile, to reduce the reflection back into the coaxial structure, the aperture radius, i.e. the radius of the outer conductor of the coaxial structure, is increased to reduce the capacitive coupling between the inner conductor and the outer conductor. Consequently, it increases the characteristic impedance of the coaxial structure and thus changes the impedance matching of the transition. However, if the length of the coaxial structure is small compared to the guided wavelength, the reflection introduced in the coaxial structure only plays a minor role and can be tuned by other design variables. In this design, the length of the coaxial section is optimized to 315μm, which is approximately one tenth of the wavelength at the center operating

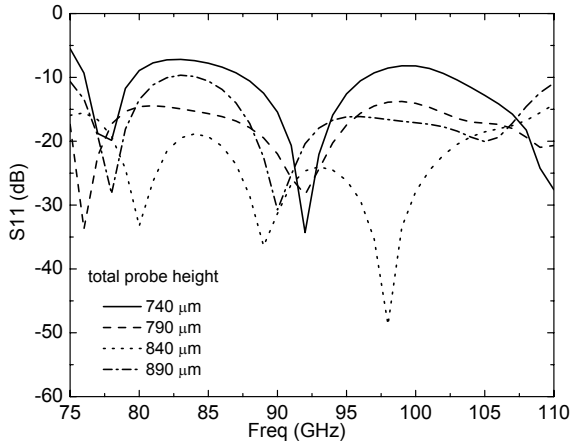
frequency. The standard WR-10 (2.54mm by 1.27mm) waveguide has been used in the transition design which is optimized over the whole of W-band. The optimized dimensions are listed in Table 3.

Table 3: Dimensions of the transition

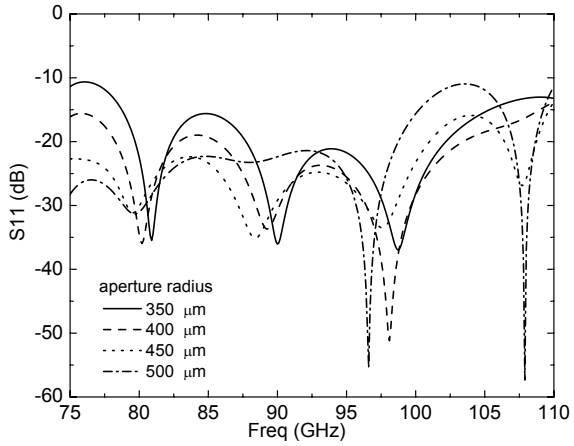
Dimensions	**Value in μm**
H_1	850
H_2	150
R_1	115
R_2	400
W_1	40
S	240
L_b	1000

In [69], an equivalent circuit model is used to explain a waveguide probe with a load at one end. In this work, the CPW tuning stub and the backshort are used to achieve wideband transition. The CPW tuning stub is shunted to the coaxial structure with characteristic impedance. The transformation provided by the transformer depends on the probe height and the offset [82]. The probe in the waveguide can be modeled as a series LC circuit. The waveguide backshort can also be represented by a shunt transmission line connected with the waveguide impedance. Although the standard WR-10 dimensions are used in this section, this approach can be generalized to other rectangular waveguide cross-sections. The probe height, the aperture radius, the length of the tuning stub, and the coaxial structure length are optimized to tune the impedance matching. The height of the probe will affect not only the capacitance and the inductance, but also the transformer. The coaxial section length is simulated using the constant probe height in the rectangular waveguide. The results are presented in Figure 39 and Figure 40.

The standard WR-10 waveguide dimensions (2.54mm by 1.27mm) are utilized for the cross section of the rectangular waveguide. The silicon layer with a coax structure is patterned on a 300-μm thick wafer. The CPW line is fabricated on top of a quartz



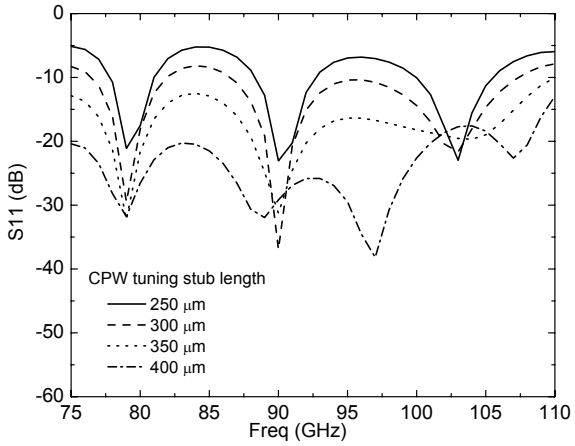
(a) Impact of the probe height.



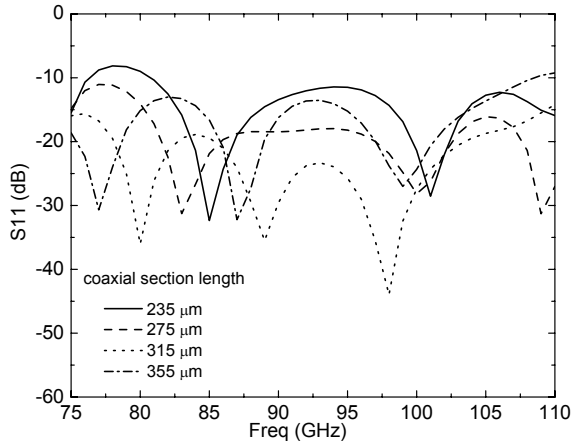
(b) Impact of aperture radius.

Figure 39: The study of parameters: probe height and aperture.

substrate. The CPW short stub is for achieving good impedance matching over wide bandwidth. The probe is located at the center of the broad wall. The design from the probe to the waveguide is based on matching the coaxial structure to the waveguide. The distance from the probe to the backshort, the height of the probe, and the radius of the probe are critical in the impedance matching. Finally, the optimized insertion loss and return loss of the transition are shown in Figure 41. An equivalent circuit of this transition from the coplanar waveguide transmission line to the rectangular waveguide is shown in Figure 42.



(a) Impact of the CPW tuning stub.



(b) Impact of coax section length.

Figure 40: The study of parameters: CPW tuning stub and coaxial section.

5.4 Fixture and Assembly

To facilitate the measurement, a back-to-back topology of the transition is designed and fabricated, shown in Figure 43. The simulated insertion loss of the back-to-back structure is between 0.87 dB and 2.68 dB over the W-band (75-110 GHz).

A fixture, shown in Figure 44, is designed to facilitate the alignment. The alignment pins are applied to provide the alignment of silicon parts. Four silicon layers are fabricated using the deep reactive ion etching technique. The aperture is patterned on this wafer. The two middle layers are etched through. The top layer is etched only

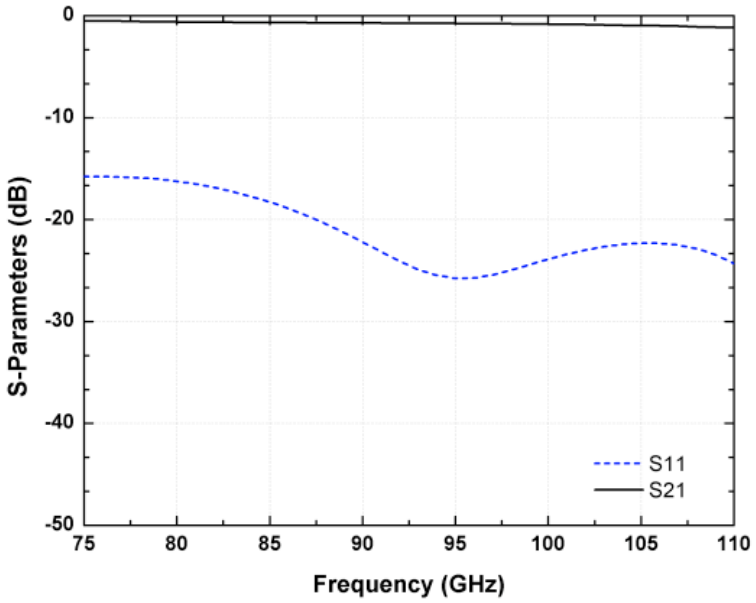


Figure 41: The simulated insertion loss and return loss of the transition.

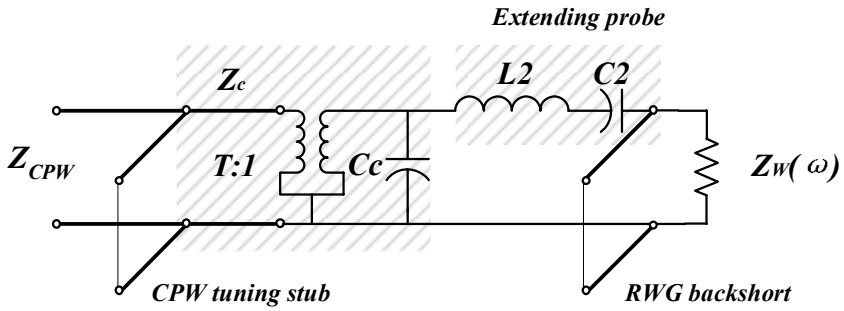


Figure 42: The equivalent of this transition.

220 μm deep with the pattern of the rectangular waveguide and released from the back. Finally, the four silicon layers form a rectangular waveguide with a 1.27 mm height. The metalized probe and the CPW line are fabricated on a quartz substrate. A picture of the fixture and the stacked samples are shown in Figure 44.

The first step of the silicon substrate preparation is wafer cleaning. Then, photoresist SRP220 is spun and patterned on the top of the silicon wafer. The patterned wafer is baked for 5 minutes, before the STS ICP is applied to etch the topside to the desired depth. A clean process is utilized to clean the photoresist residues from the

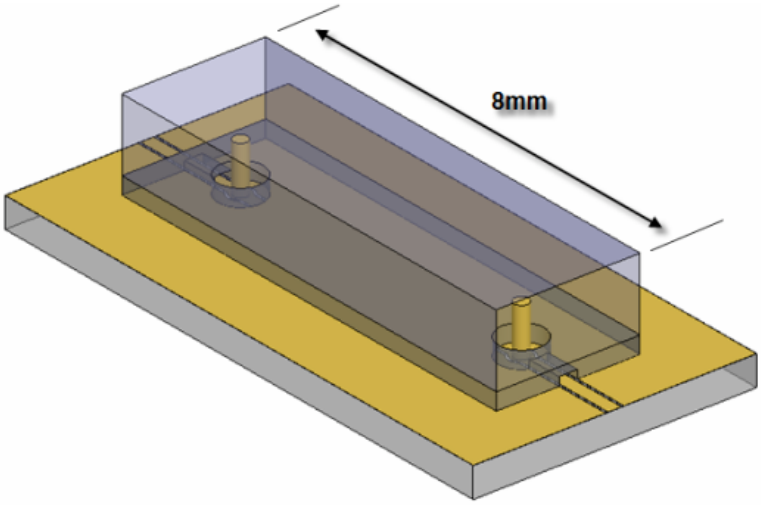
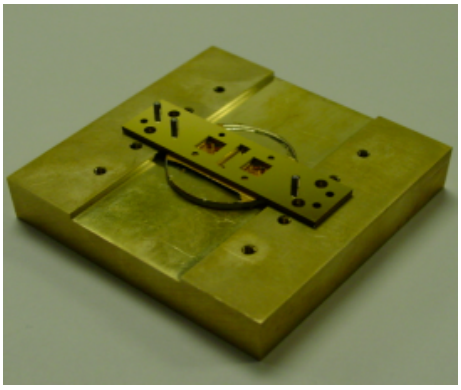
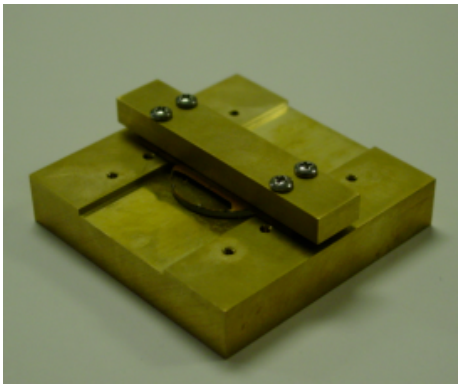


Figure 43: The back-to-back transition.



(a) The fixture, quartz substrate and silicon samples.



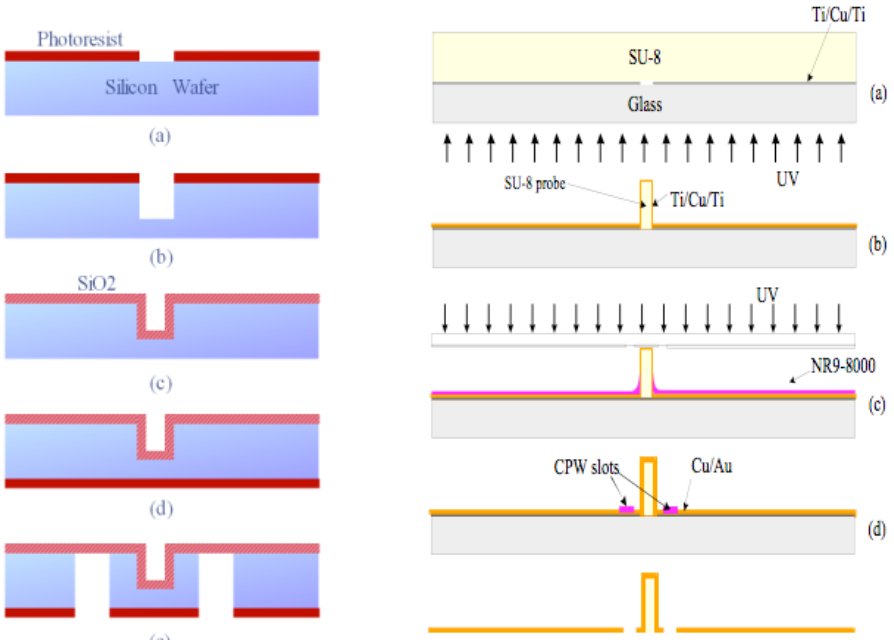
(b) The device under test.

Figure 44: The fixture and the device under test.

topside etching. Then, Uniaxis PECVD is used to deposit a thin silicon dioxide layer to protect the patterned topside. Once the silicon dioxide is deposited, the wafer is flipped and patterned with a layer of photoresist. Then, the sample is released using the dry etching. Finally, BOE is applied to remove the silicon dioxide layer. The silicon samples are metallized using a DC Sputter with a layer of Ti/Cu/Au. The fabrication flow is shown in Figure 45.

For the fabrication of the open-circuit probe, a Ti/Cu/Ti layer is sputtered and patterned to open the window for the SU-8 patterning from the backside of the

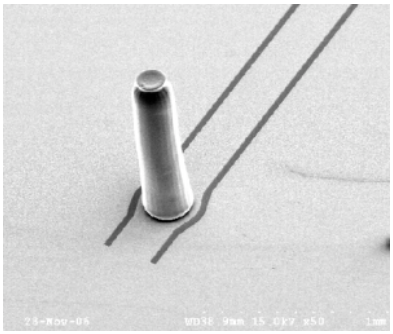
transparent quartz wafer. This improves the SU-8 adhesion to the quartz. An 800 μm negative photo-definable epoxy SU-8 2035 is dispensed uniformly on top of the quartz. It is patterned under UV to define the mold of the vertical probe. Another Ti/Cu/Ti layer is sputtered as the seed layer to cover the probes, as well as the substrate in a conformal manner. Then, the negative photoresist NR9-8000 is coated and patterned in a non-contact way to cover the CPW slot region. The copper and gold layers are electroplated to cover the sidewall of the probe, as well as the exposed ground feeding structures. As the final step, the photoresist NR9-8000 and the seed layer are removed one by one to release the structure. The fabrication flow is shown in Figure 45. Figure 46 gives the SEM images of the probe and the aperture on a 300-μm thick wafer.



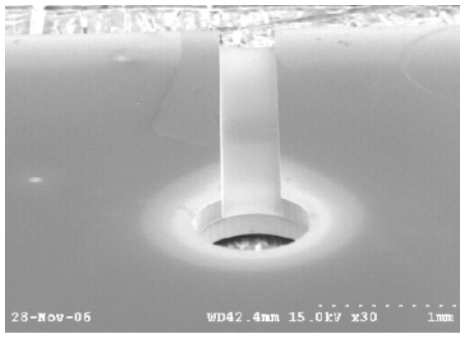
(a) Silicon process flow.

(b) SU-8 process flow.

Figure 45: The fabrication process flow. In (a), the process flow of using the deep reactive ion etching technique is given. In (b), the process of making SU-8 pillar and CPW lines on quartz is provided.



(a) SEM photo of the probe.



(b) SEM photo of the silicon sample.

Figure 46: SEM photos of the probe and the silicon sample.

5.5 Measurement

The S-parameters measurements of the waveguide transition are taken using an Agilent Vector Network Analyzer 8510XF. The NIST Multical TRL algorithm is used to calibrate the measurement system using the HP BASIC. The insertion loss and the return loss of the back-to-back structure are reported in Figure 47 and Figure 48. The measured average insertion loss of the back-to-back structure is 2.25dB with 1dB ripple and the return loss is better than 11 dB over the whole W-band. Compared to the simulation, the return loss is still higher than the simulated return loss due to the tolerance in the fabrication and assembly.

5.6 Conclusion

In this chapter, a novel fully micromachined coplanar waveguide-to-rectangular waveguide transition is presented. In the proposed transition, the CPW and the rectangular waveguide are patterned and integrated on the same side of a substrate, while the coupling probe is patterned on the substrate instead of being fabricated separately. These changes make the transition more suitable for RF packaged circuits and easily extendable to THz applications. The simulated insertion loss of the back-to-back structure is between -0.87 dB and -2.68 dB and simulated return loss is less than -16.6 dB over the W-band. The measured average insertion loss of the back-to-back

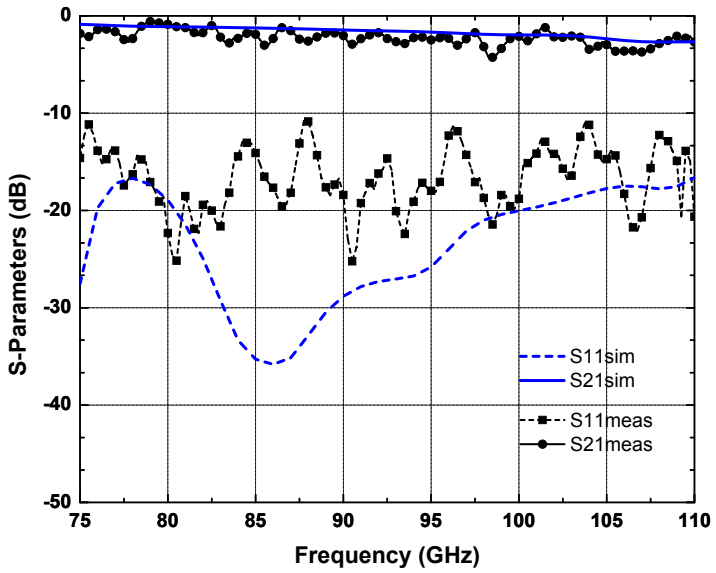


Figure 47: The measured insertion loss and return loss.

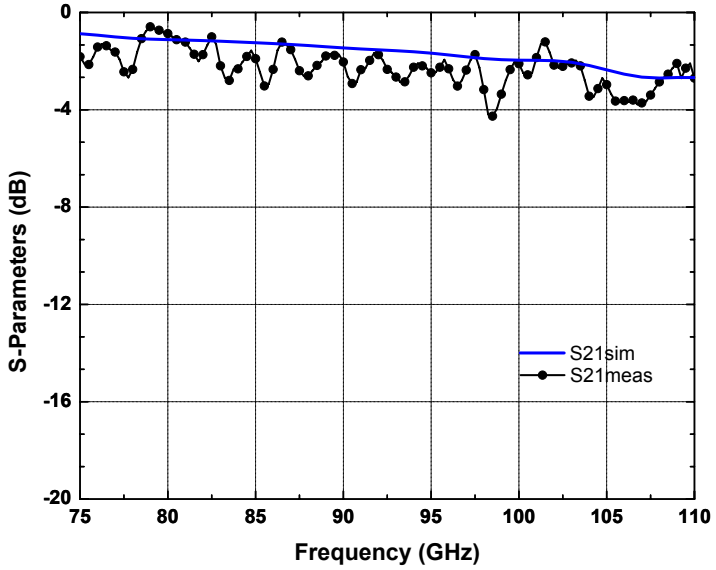


Figure 48: The measured and simulated S21 in detail.

structure is 2.25dB and the return loss is better than 11 dB over the whole W-band.

CHAPTER VI

A W-BAND MICROMACHINED CAVITY FILTER INCLUDING THE NOVEL INTEGRATED TRANSITION FROM CPW FEEDING LINES

6.1 Design Topology

This chapter proposes a W-band bandpass filter topology, shown in Figure 49, which consists of two ridge resonator structures coupled to each other. The input and output ports are produced by a direct coupling that occurs between the transition probe and the first resonant mode of the structure. The standard WR-10 waveguide dimensions (2.54mm-1.27mm) are utilized for the rectangular waveguide.

The initial goal is to design a filter with a center frequency at 96.5 GHz and a fractional bandwidth of 2.6%. The size of the resonant cavity dictates both the resonant frequency and the proximity of the input and output coupling. In the case of Chebychev filter, it is advantageous to minimize cross-coupling between the input and output ports to increase the rejection band of the filter. The separation of the ports is increasingly critical since the transition probes are located in a central region inside cavities. The filter can be fully described by the resonant frequencies of the synchronous resonators with identical dimensions, the coupling factor between two resonators, and the external coupling between the transition probes and the resonators. A drawing of all layers of the filter is shown in Figure 50.

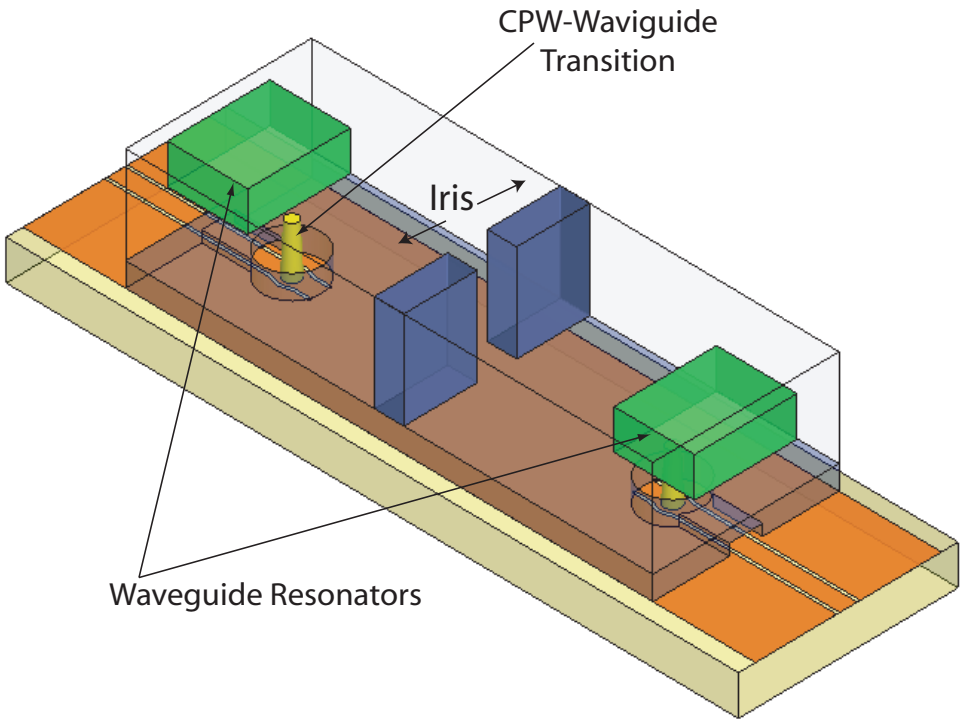


Figure 49: The proposed filter topology.

6.2 Analysis of Coupling and Resonance

The first design step is to analyze the resonance frequency of a cavity with standard WR-10 dimensions. The resonance frequency is found using the fundamental equations for rectangular waveguide cavities [68] and is given by Equation (6) and Equation (7). A standard rectangular waveguide cavity with dimensions 2.54 mm×2.54mm×1.27 mm would resonate at approximately 84 GHz. At this starting point we are facing the need to reduce the cavity size to increase the resonant frequency while keeping the largest probe separation to guarantee a good level of filter rejection.

$$K_{mnl} = \sqrt{(\frac{m\pi}{x})^2 + (\frac{n\pi}{y})^2 + (\frac{l\pi}{z})^2} \tag{6}$$

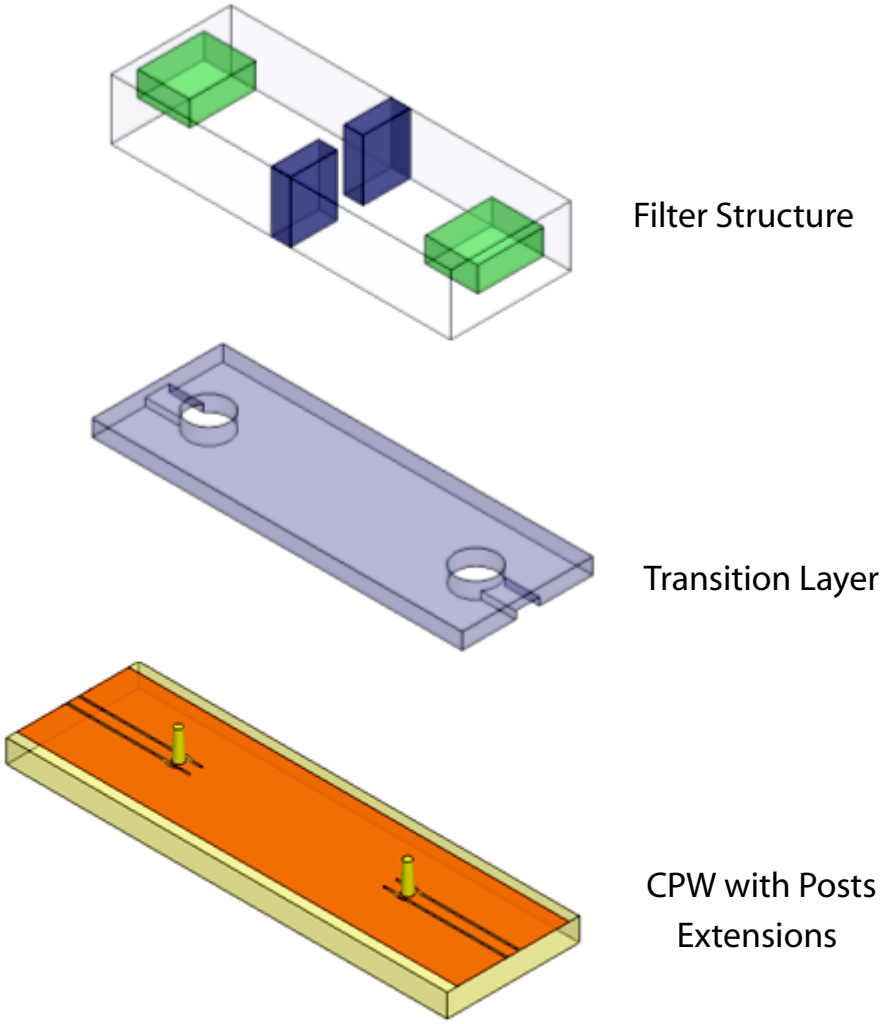


Figure 50: Transition and filter layer.

$$f_{res} = \frac{ck_{mnl}}{2\pi\sqrt{\epsilon_{eff}}} \tag{7}$$

One option is to adopt a ridge cavity design [71] [72] [73] [74] consisting of the cavity with a solid inclusive block. This gives greater flexibility in the realization of higher resonant frequencies while increasing the separation of the coupling posts. The resonator structure is shown in Figure 51. The cavity dimensions are a and b corresponding to x and z axis. The included metal block has a width W, thickness t, and length L in the x, z, y orientations respectively. The dimension t (525 μm)

is fixed as it corresponds to a silicon wafer thickness. This constrain simplifies the fabrication process.

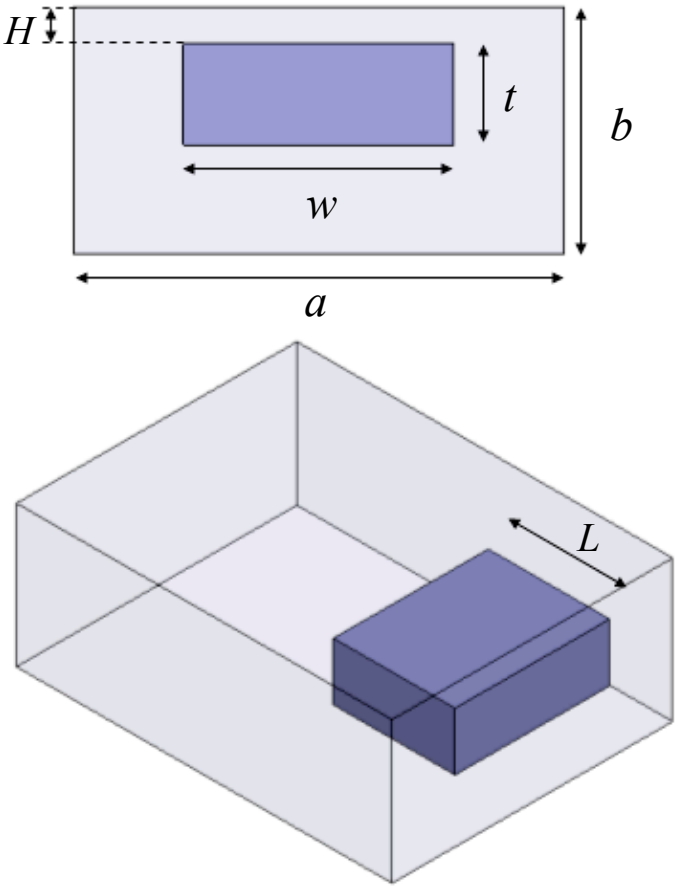


Figure 51: The dimensions of the cavity.

An eigenmode solution is conducted to characterize the cavity. The electric field distribution for the first resonant mode of the structure is shown in Figure 52. The electric field pattern can be seen with strong longitudinal component along the z axis. The field components concentrate in the region governed by the presence of the ridge component and fades with increasing $+y$. These electric field components are then used to couple to the probe of the transition placed directly below the ridge. The end of the waveguide with fading field strength allows the appropriate low coupling strength to produce a selective narrowband response.

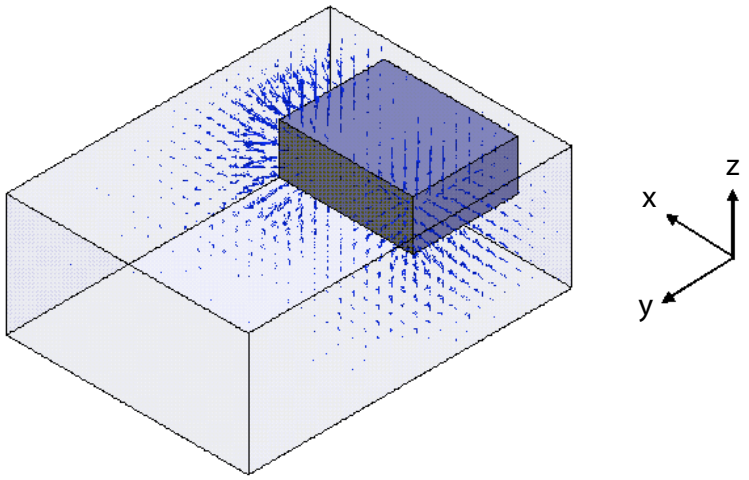
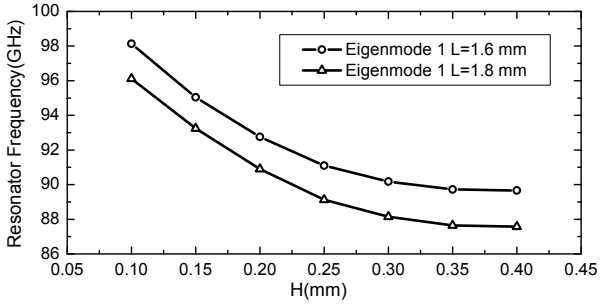


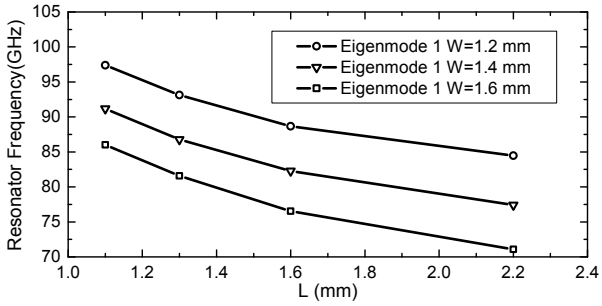
Figure 52: The E-field plot of the resonator.

In the initial analysis, the height location of the inclusive block is determined with various combinations of block sizes L and W. The results are shown in Figure 53, where the resonant frequencies are plotted versus corresponding values of H, the separation from the top of the block to the ceiling of the waveguide. This procedure is repeated for varying values of L and W and the resonant frequency is inversely proportional to the block dimension, shown in Figure 54, respectively. The presence of the internal block gives the advantages of increasing the cavity dimension along $+y$ to maximize port separation and still realize the increase in resonance frequency to the desired 96.5 GHz. In other words, when compared to a standard rectangular cavity, the current resonator with the internal block reduces the required size of the resonator needed for a specific center frequency. This size reduction is the advantage of evanescent mode filters.

The initial iris dimensions are designed by extracting the coupling coefficient present between resonators. The coupling coefficient is found by first placing the resonators in a weakly coupled configuration with respect to the input and output ports. The loaded resonant frequencies f1 and f2 are then extracted at different gap between irises. Figure 54 shows the different coupling coefficient obtained using the



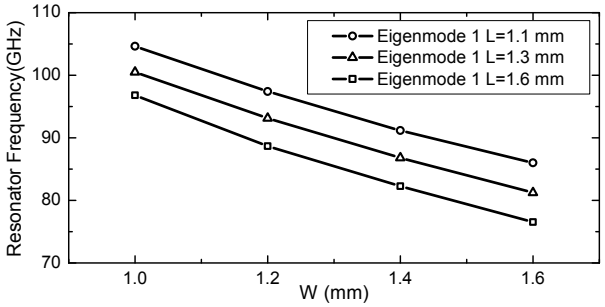
(a) Resonant frequency vs. H.



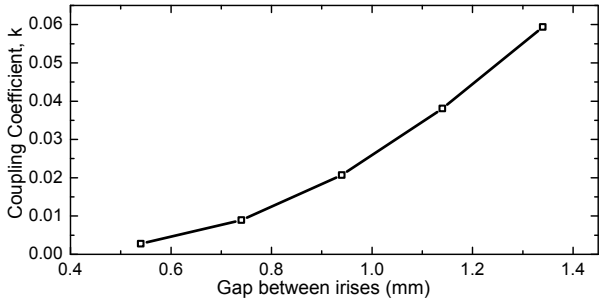
(b) Resonant frequency vs. H.

Figure 53: Resonant frequency with varying H and L.

standard equation for synchronous resonators in Equation (8).



(a) Resonant frequency vs. W.



(b) K vs. gap

Figure 54: Resonant frequency vs. W and K vs. gap.

$$k = \frac{f_2^2 - f_1^2}{f_2^2 + f_1^2} \tag{8}$$

where $f1$ and $f2$ are the frequency locations of the two resonant poles.

6.3 Implementation and Measurement

The CPW feeding and probes are fabricated on a quartz substrate. A layer of Ti/Cu/Ti is sputtered and patterned on one side. SU-8 2035 is spun and cured on top of the substrate. Then, the vertical probes are patterned under the UV light. To plate the CPW line, another Ti/Cu/Ti layer is sputtered as a seed layer. A layer of negative photoresist NR9-8000 is coated using the approximate exposure to pattern the CPW line. An electroplating process is used to plate copper/gold with a thickness of 6μm/2μm to cover the sidewall of the probe. Finally, the seed layer is released after the negative photoresist NR9-8000 is stripped. Figure 55 shows the CPW line, probe, and a silicon sample in detail. The deep reactive iron etching (DRIE) technique is used to fabricate silicon layers, shown in Figure 56 (a). The bottom layer is made with a 300-μm thick wafer. The two middle layers are fabricated using 525-μm thick wafers. The top layer is etched only 220-μm deep and released from the back with different patterns. A photo of the fixture and two middle layers on the quartz substrate is shown in Figure 56 (b).

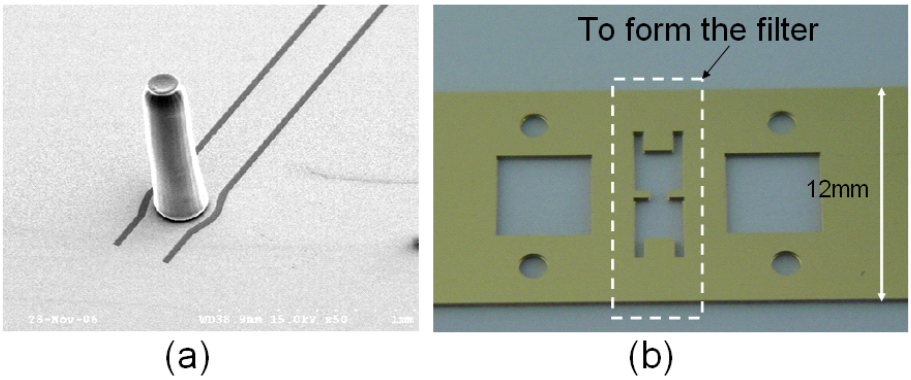


Figure 55: (a) The probe and CPW. (b) Silicon layer in detail.

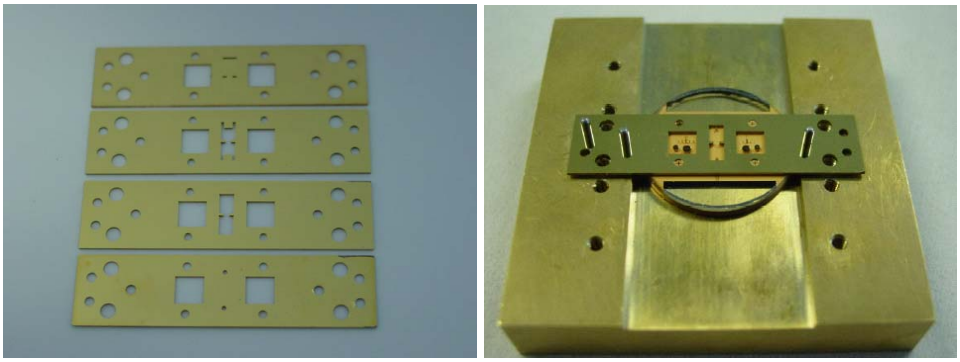


Figure 56: (a) Four silicon layers to form RWG and filter. (b) Two stacked silicon layers on fixture.

The silicon wafer is cleaned and then patterned using the photoresist SRP220. STS ICP is employed to etch the patterned silicon to the desired depth. Then, the wafer is cleaned and Unaxis PECVD is used to deposit a thin silicon dioxide layer to protect the etched topside. Once the silicon dioxide is deposited, the wafer is flipped and patterned on the backside using SRP220. The silicon sample is released using STS ICP through etching the wafer from the backside. The diluted HF is used to remove the silicon dioxide layer. The silicon samples are sputtered using DC-Sputter for 7-μm thick Ti/Cu/Au layer.

The filter presented in the chapter is simulated using full wave simulator, Ansoft's HFSS 10. The quartz substrate has the dielectric constant of 3.78 and the loss tangent of 0.0002. The metal on the quartz substrate and on the silicon wafers is gold with the conductivity of 4.1E7 Siemeons/m. The simulation result is reported in Figure 57. The filter has a center frequency of 96.5 GHz with 2.6% bandwidth. The simulated insertion loss in the passband is 2.5 dB.

The measurements at W-band are taken using an Agilent Vector Network Analyzer (VNA) 8510XF. The VNA is calibrated using NIST MultiCal thru-reflect-line (TRL) algorithm. A pair of probes with 250 μm pitch are used in the measurement. The measured passband insertion loss is 4.14 dB. The two poles are located at 96.3 GHz

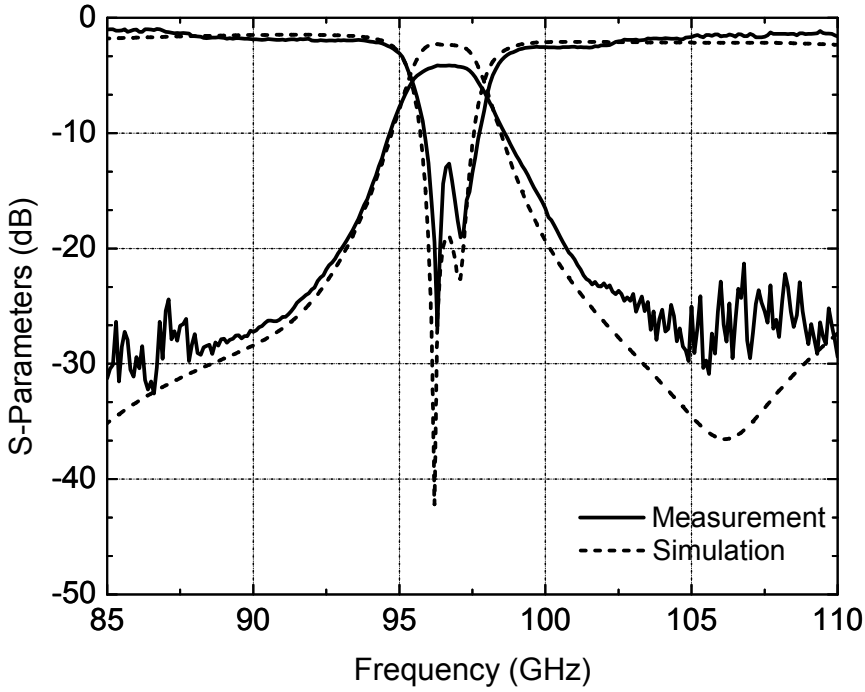


Figure 57: Simulation and measurement results of band-pass filter with transitions.

and 97.1 GHz in the return loss. The measured filter has the center frequency of 96.6 GHz with a bandwidth of 2.9%. Compared to the simulated data with 2.5 dB loss in the passband, the measured filter has 1.64 dB additional loss. The bandwidth is increased by 0.3%.

The additional loss may come from the assembly tolerance, the surface roughness of the silicon waveguide sidewall, and the gap between the layers. The tolerance of micromachining including DRIE, photolithography and metallization is on the level of μm or less in the class 100 cleanroom. However, the tolerance of alignment pins determined by the machine shop is on the level of mil (1/1000 inch or 25.4μm). To allow the relaxed tolerance on the alignment pins in the assembly, the holes on the four layers of silicon samples are made slightly larger than that of the alignment pins. A rigorous sensitivity analysis of coupled resonator filter can be found [75].

Unfortunately, we can not directly use it since the tolerances in the assembly will affect not only the coupling, but also the impedance matching of the transition.

The simulation results in Figure 58-Figure 59 show the sensitivity of the response to the horizontal displacement of the silicon layer having the internal block. y denotes the displacement along the CPW lines. x denotes the displacement in perpendicular to the CPW lines. The filter is simulated while sweeping the displacement along y and x. The simulation shows the filter response is very sensitive to the displacement in parallel to the CPW line since the electric field is changed in this direction through the presence of the probe that is right below the block and close to the edge. To reduce the loss from assembly, a non-standard waveguide with less height will be helpful. It will not only reduce the necessitated layers, but also simplify the transition design since the waveguide impedance is proportional to the height. An alternative solution is to adopt the pin-free alignment method. For applications with an operating frequency higher than W-band, or even in the THz range, a shorter wavelength makes the stacking approach easier because fewer silicon layers are needed.

The surface roughness on waveguide sidewalls comes from the deep reactive ion etching process. The surface roughness, although hard to avoid, can be further reduced by adjusting the fabrication parameters, such as the power, time and flow rate of the gases in the etching and passivation cycles. Another possible reason for the additional loss is the gap between the stacking wafers. Instead of cutting the waveguide along the center of the broad wall, the stacking technique may break current along the sidewall if a gap exists. In our experiment, a metal cover with four screws is used to tight the stacking wafers up. In the future, the thermal bonding technique can be employed to prevent the gap.

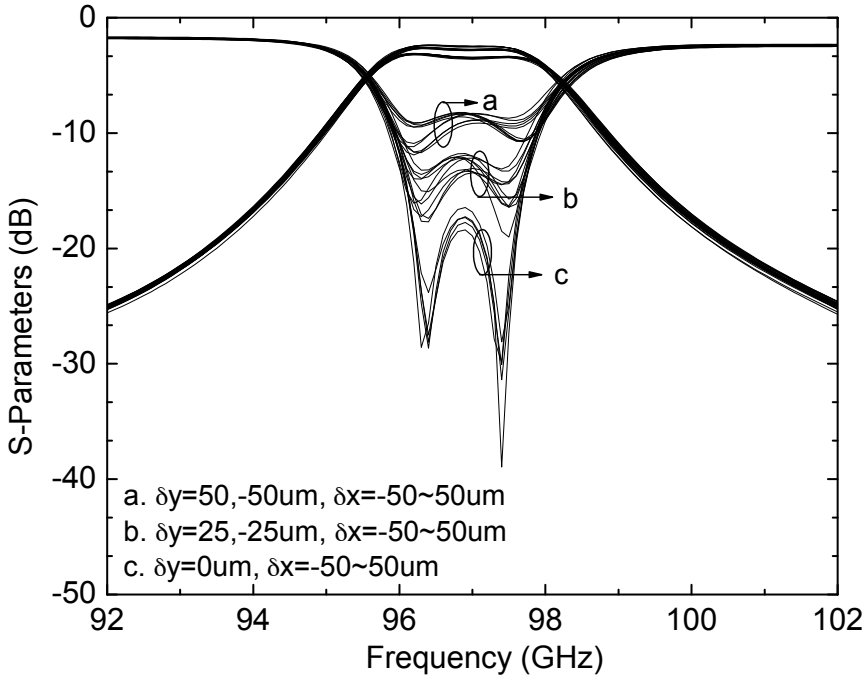


Figure 58: Simulated filter with transitions response versus frequency when the second silicon layer undergoes displacement.

6.4 Conclusion

This chapter presents a novel CPW to rectangular waveguide transition as an enabling structure for the integration of a W-band filter [76]. The proposed transition has several advantages: the CPW and the rectangular waveguide are patterned and integrated on the same side of the substrate; the coupling probe is patterned on the substrate instead of being fabricated separately. These advantages make the transition more suitable for RF packaged circuits and easily extendable to THz applications compared to the existing approaches. The metalized probes in the proposed filter design are adopted to couple the signal from the CPW line to the waveguide resonant cavities of a 2-pole filter and eliminate the need for waveguide input/output ports. The measured filter response agrees well with the simulated response.

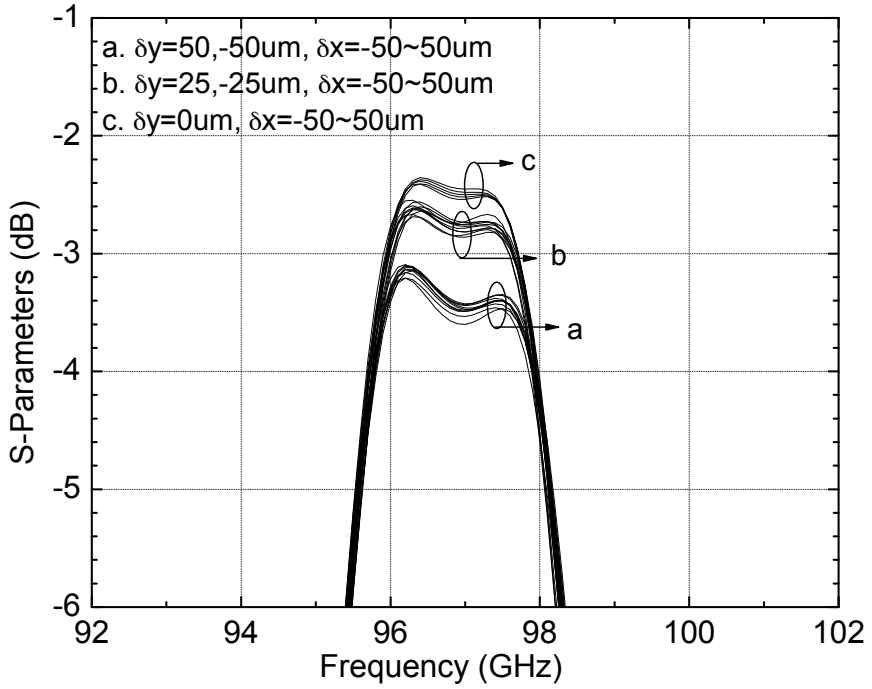


Figure 59: The detail in the passband of simulated filter with transitions response versus frequency when the second silicon layer undergoes displacement.

CHAPTER VII

A HIGH-Q CAVITY RESONATOR AND FILTER FOR RECONFIGURABLE WPAN APPLICATIONS AT 60 GHZ

7.1 Introduction

In this chapter, a novel silicon micromachined high-Q cavity resonator at 60 GHz is presented. The concept of the proposed high-Q resonator is introduced first. The novel realization of the cavity resonator is demonstrated through silicon micromachining techniques. Full-wave simulations are conducted to verify the propagation mode and the resonant frequency. The resonant frequency of the cavity resonator can be tuned through changing the length of a planar stub shunted to a current probe in the cavity. Experimental results validate the simulation and show great Q factors which are over 320 at the resonances for the wireless personal area network applications.

A high-Q resonator is highly valued in reconfigurable wireless communication systems. The cavity resonator [77]- [80] has the intrinsic superior quality factor and power handling capacity over its planar counterparts, e.g. microstrip resonators and coplanar waveguide resonators.

However, the resonant frequency of the cavity resonator is traditionally tuned either by mechanically inserting a screw [81] or by adjusting the gap between a capacitive post and the ceiling of the cavity through piezoelectric materials [82], shown in Figure 60, or mechanical force [83]. These methods are difficult to integrate with monolithic microwave circuits and are not feasible for low-cost wireless personal area network applications at 60 GHz.

In the last two decades, with the advance of micromachining techniques and ferroelectric materials, RF MEMS switches [84] and Barium Strontium Titanate (BST)

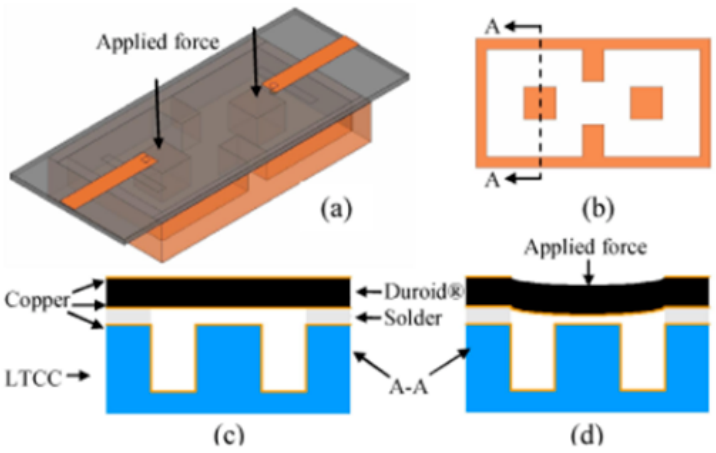


Figure 60: Existing tunable cavity filter [82].

capacitors are widely used in planar resonators and planar filters. Tunable planar filters using RF MEMS switches have been presented with third-order intermodulation intercept point over 40 dBm [85] and remarkable reliability of over 100 billion cycles [86]. The BST-based capacitors have shown great switching time on the nanosecond level [87] and continuous frequency tuning capability. The pin diodes are extensively utilized in planar circuits and have the advantages of low cost, fast switching speed and low tuning voltage. Although RF MEMS switches, BST capacitors and pin diodes have been successfully demonstrated in the integration with planar monolithic microwave circuits either printed on a substrate or elevated in the air with the support of a membrane, a low Q factor is associated to these planar passives. In this chapter, a novel high-Q cavity resonator is presented at 60 GHz. The resonant frequency of the cavity resonator can be tuned by changing the length of a shunt planar stub. Therefore, the tuning components, RF MEMS switches, BST capacitors or pin diodes, can be employed to change the electrical length of the stub and to tune the resonant frequency of the cavity resonator. The successful demonstration of the cavity resonator will be beneficial to building reconfigurable cavity-based wireless communication front-ends with high-Q factors at 60 GHz. The concept of the novel cavity resonator is described first. Then, the realization of resonator is introduced

and is verified using full-wave simulation software. The fabrication and assembly of the resonator is presented shortly. Finally, the experimental results are presented and discussed.

7.2 Tunable Cavity Resonator Concept

The cavity resonator is enclosed by the metalized substrate, lid, sidewall, and current probe. In contrast with the conventional micromachined cavity resonator, this resonator has a slot on the sidewall next to the current probe. On the substrate, a planar stub is shunted to the current probe and is isolated from the metalized substrate by an encompassed gap. The shunt stub starts from the current probe and extends out of the boundary of the cavity sidewall. Figure 61 depicts the topology of the proposed tunable cavity resonator. The conventional cavity resonator has the resonant frequency determined through Equation (9).

$$f_{mnp} = \frac{c_0}{2\pi\sqrt{\epsilon_r}}\sqrt{(\frac{m\pi}{d})^2 + (\frac{n\pi}{b})^2 + (\frac{p\pi}{g})^2} \tag{9}$$

where d, b and g are the width, height and length of the cavity resonator respectively, c_0 is the speed of light and ϵ_r is the dielectric constant of the cavity filling. The resonant frequency of this resonator is primarily determined by the volume enclosed by the sidewall and the current probe when the slot is small and the current probe is close to the slot. The slot, the current probe and the shunt stub serve as a perturbation of the cavity resonator. The resonance frequency shift comes from the susceptance change induced by the length of the shunt planar stub. The resonant frequency of the cavity resonator decreases when the length of the shunt planar stub increases.

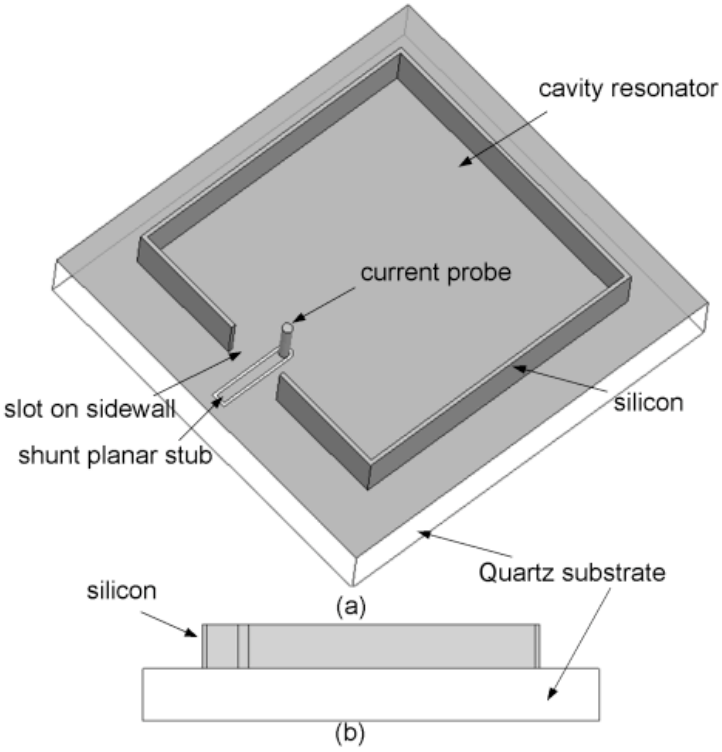


Figure 61: The proposed tunable cavity resonator.

7.3 Micromachined Realization

The proposed cavity resonator is very attractive for reconfigurable applications. In this chapter, three shunt planar stubs with different lengths demonstrate three different resonant frequencies. The electric field distribution of the fundamental TE_{101} mode in the cavity is simulated using Ansoft's HFSS and the result is shown in Figure 62.

The cavity resonator is fed through coplanar waveguide (CPW) transmission lines which are deposited on top of the substrate. These two feed lines enter the cavity through two openings on the sidewalls next to the sidewall with a slot. They are weakly coupled to the resonator for accurately extracting the unloaded quality factor from the resonant response. To validate the concept, a micromachined cavity resonator is designed at 60 GHz for WPAN applications, shown in Figure 63. The dimensions of the tunable resonator are presented in Table 4. The resonant frequency

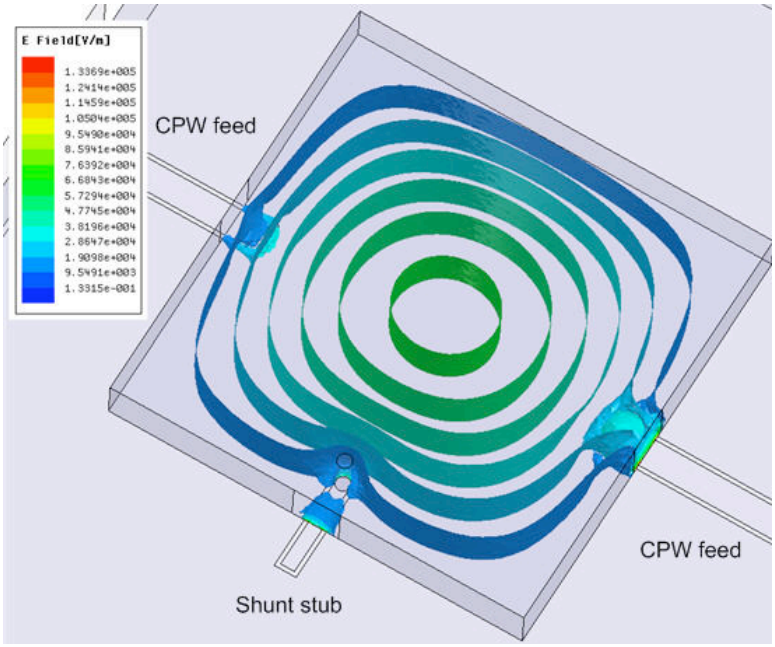


Figure 62: The E-field of the cavity resonator.

is tuned by the length change of X_t. Three resonators are made with same dimensions, except X_t, to show the frequency tuning. The 'state 1' of the resonator denotes that X_t is 600μm; the state 2 that X_t is 800μm; the state 3 that X_t is 1000μm. Figure 64 gives the implementation of this tunable cavity resonator using micromachined techniques.

Table 4: Dimensions of the proposed resonator

Variable	**Vaule(μm)**	**Variable**	**Vaule(μm)**
$S1$	240	Yf	1900
$W1$	35	Ys	1000
$S2$	120	Yi	1780
$W2$	35	R	60
Xc	3600	Hc	310
Yc	3560	Xt	600(state 1)
$G1$	400	Xt	800(state 2)
$G2$	60.58	Xt	1000(state 3)
Hs	60.58		

The lid, the sidewalls and the current probe are made by using a micromachined

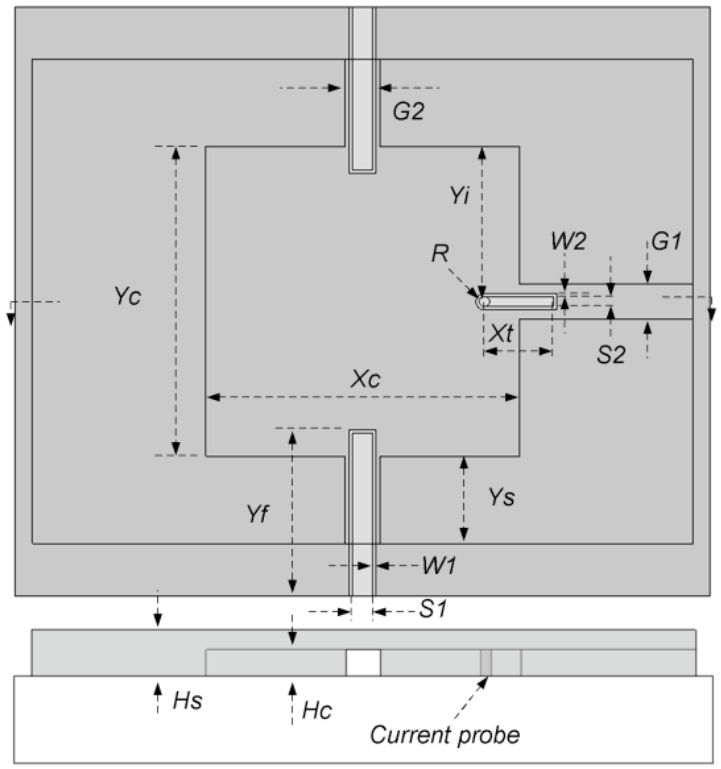


Figure 63: The dimensions of the cavity.

silicon sample. The shunt stub and two CPW feed lines are deposited on a quartz wafer. The whole cavity is formed by bonding the silicon sample to the quartz wafer. To ease fabrication, the height of the cavity is chosen to be 310 μm. A higher quality factor can be reached by increasing the height of the cavity.

7.4 Implementation and Assembly

The entire resonator is built using micromachining techniques on a quartz wafer and on a silicon wafer. The quartz wafer used in this chapter has an 1-inch diameter, which is big enough for two dies, one die for each resonator, shown in Figure 65. The two dies on one quartz wafer have same dimensions except the length of X_t.

A quartz wafer was cleaned first with Acetone. A photoresist layer was spun and patterned on top of the quartz wafer. A lift-off process was carried out by using electrical beam evaporator to achieve a metal layer, Ti/Cu/Au, with a total

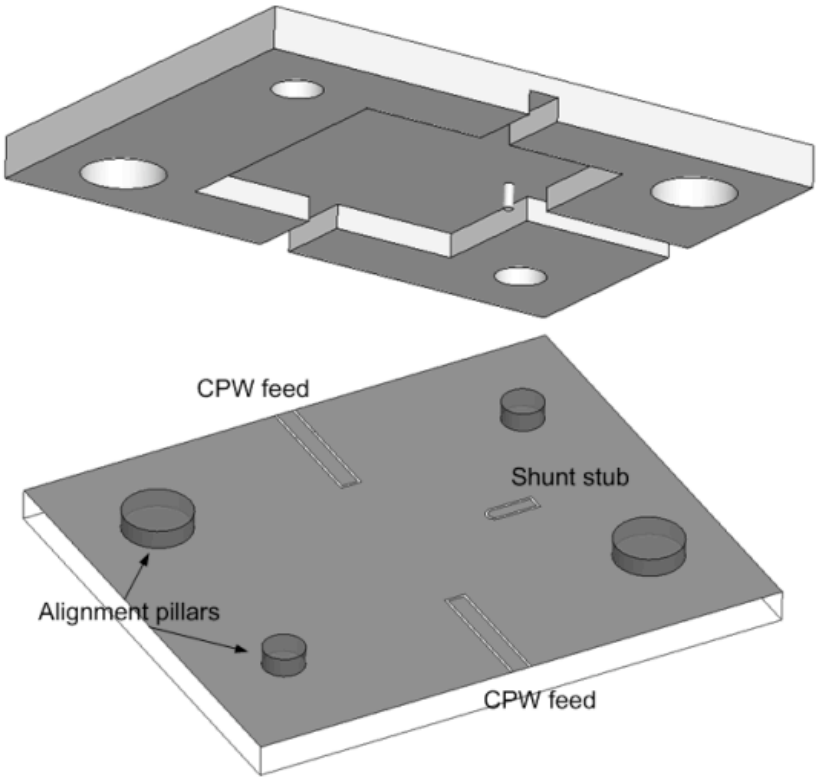


Figure 64: The implementation of the cavity.

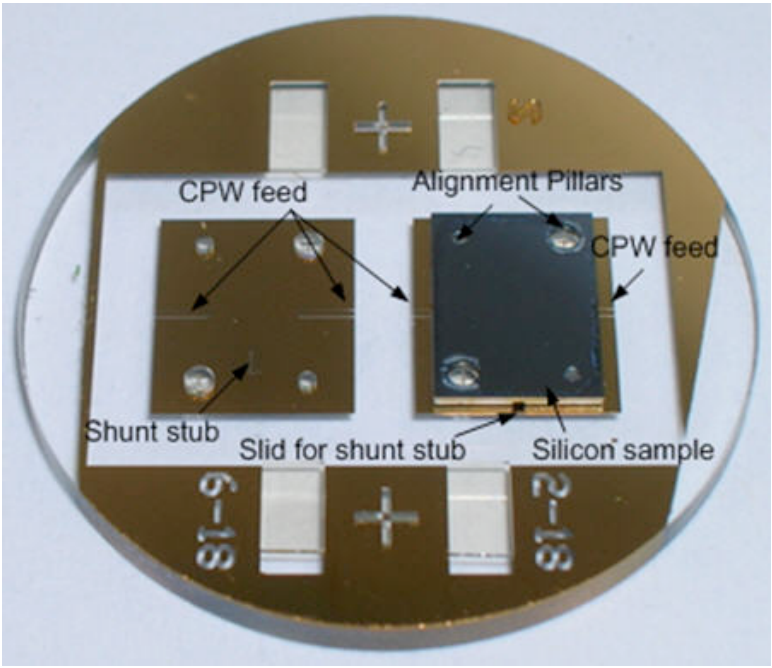


Figure 65: Quartz wafer with two dies, the right one assembled with silicon sample.

thickness of 3 μm. The lift-off process improved the surface roughness of the metal layer compared to electroplating. The metal layer that had the CPW feeds and shunt stub on it served also as the metal bottom of the cavity. The alignment pillars were made on top of the metal layer using negative photoresist SU-8 with a height of 150 μm. These alignment pins were used to accurately align the silicon sample on the quartz wafer. In Figure 65, the silicon sample was assembled on the right die.

The silicon sample shown in Figure 65 was made using deep reactive ion etching techniques. More than twenty silicon samples were obtained from one four-inch wafer. First, a photoresist layer was spun and patterned on the silicon wafer to form a mask for deep etching. An inductive coupled plasma tool, STS ICP, was used for deep etching. After removal of the photoresist residue, a thin silicon dioxide layer was prepared as a stop layer for the backside etching. Then, the etched wafer was flipped, patterned, and etched from the backside to release the silicon sample. The DC-sputter was used to put down a 3-μm layer of Ti/Cu and a 100-nm layer of Au on the cavity side after the removal of the photoresist residue and the thin silicon dioxide layer. The SEM picture of the silicon sample in Figure 66 was taken using a Hitachi 3500H SEM. The height of the cavity was measured using a Tencor KLA Profilometer. A four-degree re-entrant angle on the sidewall from the deep etching is noticed in the SEM image. The cavity volume is increased and the resonant frequency is decreased due to the re-entrant angle. Finally, the silicon sample and the quartz wafer were assembled together and mounted on a fixture to prevent the air gap between them.

7.5 Experiment and Discussion

The measurements of the tunable cavity resonator were taken using an Agilent Vector Network Analyzer (VNA) 8510XF and GGB probes with 250-μm pitch. The Short-Open-Load-Thru (SOLT) calibration method was used to calibrate the VNA to the probe tips. The measured resonant frequency of the resonator at each state, shown

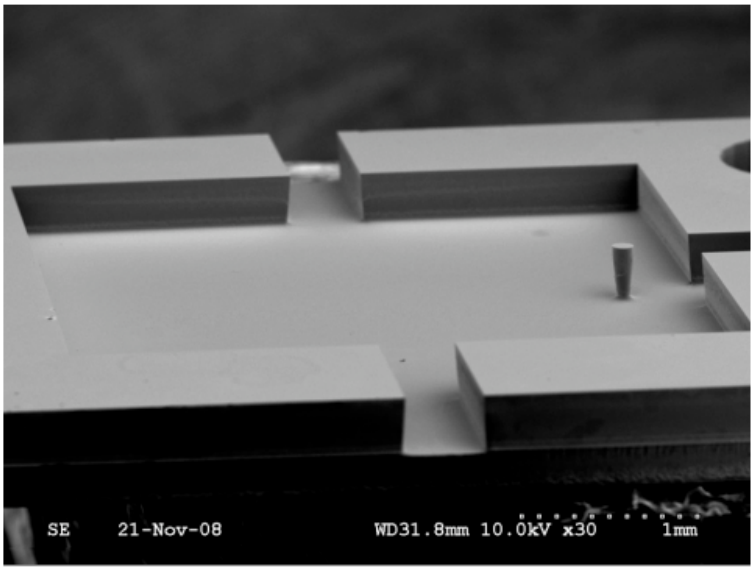


Figure 66: SEM picture of the silicon sample.

in Figure 68, has very good agreement with the simulated results. Ansoft's HFSS is used in the simulation, where the conductivity of the copper is 5.8×10E7 S/m, the loss tangent of the quartz wafer is 7×10E4, and a four-degree re-entrant angle is included. The loaded Q and unloaded Q of the resonator are calculated using the equations in [80] and reported in Table 5. The measured unloaded Q is 328 at 'state 1', 368 at 'state 2' and 356 at 'state 3', which are lower than those in the simulation shown in Figure 67 and Figure 68. This is probably due to the surface roughness of the cavity. However, the concept of the cavity resonator with the resonant frequency affected by a current probe and a planar stub with an additive length is validated with Q over 320. The summary of the measured and simulated values are reported in Table 5.

Table 5: Simulated and measured resonant frequency and unloaded Q.

State	Simulation			State	Measurement		
	f_0	Q_l	Q_u		f_0	Q_l	Q_u
1	60.58	336	395	1	60.44	298	328
2	59.77	379	453	2	59.69	331	368
3	59.23	376	448	3	59.27	316	356

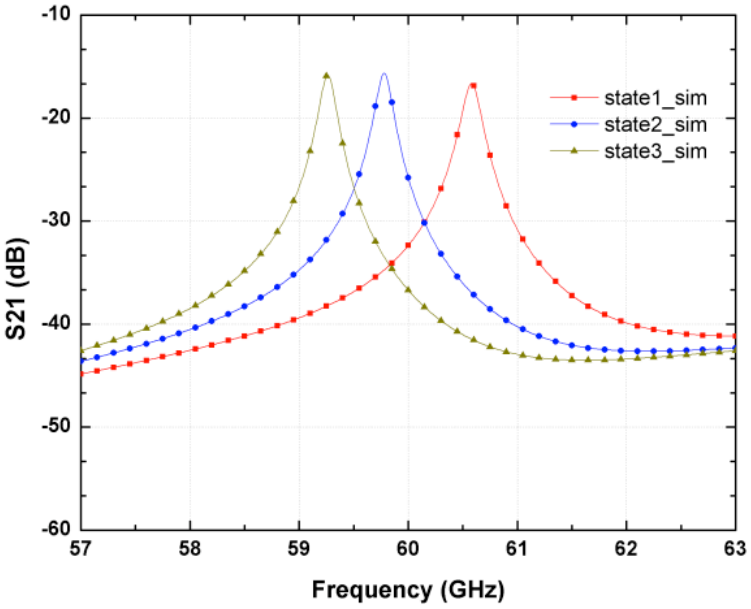


Figure 67: Simulation of the cavity resonator.

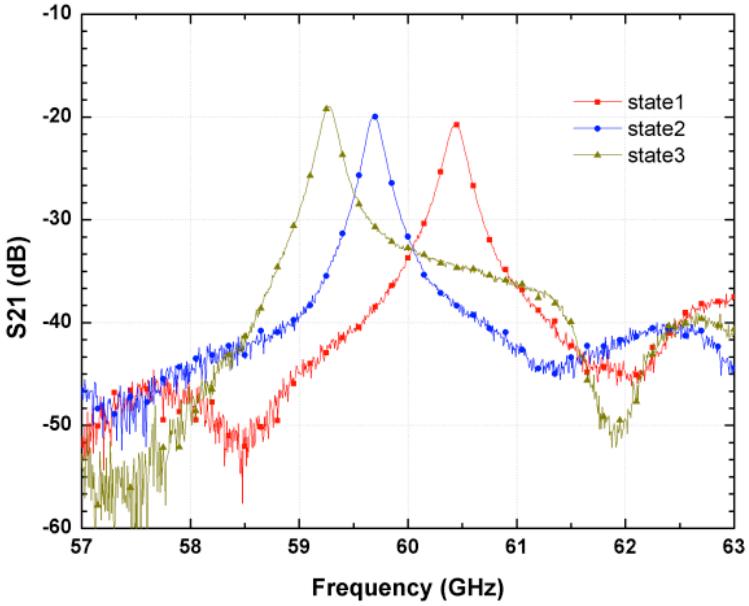


Figure 68: Measurement of the cavity resonator.

7.6 Conclusion

In this chapter, a novel cavity resonator with a current probe and a planar shunt stub is presented. The proposed cavity resonator scheme provides the opportunity of using planar tuning components, RF MEMS switches, BST capacitor or pin diodes, to build

reconfigurable wireless communication systems based on a cavity-based resonator that has intrinsically high-Q factor over its planar counterparts. The measured resonant response shows great agreement with the simulation results. The measured unloaded Q is over 320 for all three states at the resonant frequencies around 60 GHz.

CHAPTER VIII

A BROADBAND 900-GHZ SILICON MICROMACHINED TWO-ANODE FREQUENCY TRIPLER

8.1 Introduction

Terahertz (THz) signal sources in the 100 GHz to 10 THz have attracted scientific interests over several decades for both terrestrial and astronomical applications [5]. The abundant THz radiation that bathes our universe contains a wealth of scientific information, such as, the dynamic properties of a wide range of molecules on planets in our solar system as well as in remote regions of the universe. The spectroscopic signatures of such molecules allow scientists to build dynamical models that help to better our understanding of the universe. The investigation of the correlation between the shape of the ozone hole and the distribution of chlorine monoxide tackles the puzzle of how human activities affect the health of our planet [88].

A superheterodyne radiometer is a crucial instrument for conducting quantitative spectroscopy on space missions. An important component in such instruments is the THz signal source used to pump mixers in a superheterodyne radiometer. THz signal sources that are compact, highly efficient, broadband and low-cost are extremely desirable. A couple of decades ago, tube-type THz signal sources, known as the gas-filled and vacuum tube, including backward wave oscillator, gyrotron, klystron, and far-infrared laser, were intensively studied [89], [90].

Solid-state devices provide a compact and lightweight solution for generating THz radiation. Although rapid advance has been made in HBV diodes [91], [92], [93] and three-terminal solid-state devices such as high electron mobility transistors [94]

and heterojunction bipolar transistors [95], GaAs Schottky diodes still provide unsurpassed performance advantage and are widely used in the THz frequency multipliers [5], [96], [97].

Schottky diode chips are nominally housed in waveguide based circuits to provide appropriate input and output matching conditions along with providing a well understood radiatin mode. Normally, these waveguide circuits and their fixtures are fabricated with the use of direct machining, including high precision lathes and milling machines and they have been demonstrated up to approximately 2 THz [98]. However, as the desired wavelength is increasingly small in the THz band, the small dimensions make these waveguide circuits difficult or impossible to fabricate and the cost of fabrication often becomes prohibitive in direct machining. The direct machining process is also constrained by the diameter of milling tools that lead to round corners. An example of direct machining is a 2.5 THz corrugated horn that is reported in [99] with the miniature being 27μm$\times 105\mu$m. Other direct machined waveguide circuits include frequency multipliers [91], [100] and power combining circuits [101], [102].

Besides direct machining, many other techniques have also been proposed to provide low-loss and low-cost solutions for the fabrication of THz waveguide circuits [99], [103]. Electroforming relies on electroplating to form a metal layer onto a mandrel in a plating bath. The metal layer is eventually built up in the bath and an independent shape forms. The mandrel is then burned out, leaving the expected metal waveguide structures. The electroforming process is suitable for producing complex waveguide structures, but the process is fairly time consuming and requires a high-precision mandrel first. An example of electroforming is a 2.5 THz horn reported in [104] with the use of a standard copper electroforming process.

Surface micromachining with the use of thick photoresists, such as, SU-8, to build the structure of THz wavguides has also been reported [105]. A thick photoresist layer can be spun and patterned for a thickness of up to 1-2 mm. The developed SU-8 is then

metalized to form waveguide structures. The fabrication of SU-8 is relatively simple, but has a long baking and curing time determined by the height of the structures. The uniformity of the height over a large area, e.g. a 4" wafer, is strongly affected by the baking and curing recipe. The direct use of SU-8 as dielectric filling to form a waveguide structure leads to high loss at THz frequencies. Therefore, SU-8 is suitable for sidewall structures. Instead of using thick photoresist as a structure layer, metal-film waveguides use thick photoresist as a sacrificial layer [103]. Once the thick photoresist structure forms, a thin metal layer is sputtered as a seed layer, followed by an electroplating process to have a thick metal layer. The thick photoresist is removed by chemicals, leaving a waveguide structure filled with the air. The metal-film process is capable of building the full-height waveguides only at the high end of THz frequencies because of the limit of photoresist thickness. A reduced-height waveguide horn antenna is reported in [106] at 200 GHz.

Unlike surface micromachining with the use of photo-definedable polymer, a stereo-lithography technique, extensively studied in the millimeter-wave range, is a 3-D fabrication method that uses laser beam to cure resin material layer by layer [107], [108]. The entire waveguide structures are immersed in resin, therefore the stereo-lithography method is for stand-alone components and is not compatible with the standard CMOS process. X-ray LIGA is a complex process, allowing to achieve extremely high-aspect-ratio structures in the positive resist. This process requires a thick X-ray mask and is an expensive method. X-ray LIGA can produce nearly perfect geometries. The X-ray LIGA process is introduced in [109] to acheive a 600-700-GHz backward wave oscillator with the feature size of about 20 microns.

Without using any photoresis or resin, laser beam etching has been proposed to drive silicon etching using chemical reactions. A laser-assisted chemical etching system is summarized in [110]. The Cl_2 gas is used to accelerate the etching process. The laser beam etching method is capable of achieving highly complex 3-D structures

in a small area of several square millimeters. This method is time consuming to etch a chunk of silicon substrate because it is a process in series and a layer of 1-2 μm thick silicon is usually removed along with the moving of the laser beam. The fabrication of laser beam etching requires a blank wafer to avoid the contamination of the etching chamber and the corrosive effect of ambinet Cl_2. In [111], a 2-THz waveguide structure is reported using the laser beam chemical etching technique at the University of Arizona. This technique also becomes problematic for the lower THz range where feature sizes can be relatively large.

The wet etching of silicon is a simple technique and has been widely used in waveguides [112], filters [113], antennas [114], and mixers [115]. However, the design is limited by the crystal orientation of silicon substrates and accurate dimensional control is also difficult. Deep reactive ion etching technique is a dry etching technique that is powered by inductively coupled high-density plasma and can achieve a high aspect ratio up to 20:1. This technique has been used in a wide range of millimeter-wave components, including the finite coplanar line-to-waveguide transition [116] and the waveguide hybrid junction [117]. For the submillimeter-wave passives, a 400-GHz straight waveguide [118] and a 325-500-GHz quadrature hybrid with waveguide structures [119] were reported. For THz signal sources, a silicon micromachined waveguide multiplier using the heterostructure barrier varactor was reported at 261 GHz in [120]. A 600-GHz mixer using both wet and dry etching was presented in [121].

The purpose of this study is to investigate the feasibility of using the deep reactive ion etching technique as an enabling integration method to build THz frequency multipliers at 900 GHz. Initially developed in the semiconductor industry, the deep reactive ion etching technique is friendly to mass production, inherently suitable for high-precision design, indiscriminately attainable to all types of silicon substrates with different doping and crystal orientations. The waveguide passives fabricated using this technique have the intrinsic properties of low-loss, high-Q, and high power handling

capacity. In this study, a broadband 900-GHz silicon micromachined frequency tripler using a pair of Schottky diodes in the balanced configuration is successfully demonstrated for the first time. The outline of the remaining chapter is as follows: Section II introduces the circuit design. Section III describes the fabrication and assembly of the compact waveguide circuits. The measurement and analysis are presented in Section IV, and finally, conclusion is given in Section V.

8.2 Circuit Design

8.2.1 Design Methodology

The 900 GHz tripler chip utilizes topology shown in Figure 69 and previously reported in [122], [123], [124]. As in [122], monolithically integrated input and output probes have been added to simplify assembly. Mettalic on-chip beamleads allow for the mounting and handling of the chip inside the waveguide block.

Since 1990s, the advance of full-wave electromagnetic simulators, e.g. Ansoft's HFSS, and nonlinear circuit simulators, e.g. Agilent's ADS, have greatly aided in the design of broadband multipliers. Pioneered by [123], the simulation was performed with the ever increasing accuracy and speed, thanks to the rapid progress of both software and the hardware. Passive 3-D structures and discontinuities are simulated and de-embeded using full-wave simulators and the optimized S-parameter files are extracted. The S-parameter files are imported into ADS to optimize the performance of frequency multipliers for maximizing output power and conversion efficiency with the use of electrical and physical parameters of Schottky diodes.

The waveguide structure of the tripler is split in half along the E-plane center and the two half blocks have the mirrored patterns. The GaAs chip with metal beamleads is mounted onto the micromachined waveguide chip channel. The diodes in this design are self-biased and thus do not require a dc biasing scheme, though , the metal beamleads provide RF ground for the circuit in this design. The two anodes are

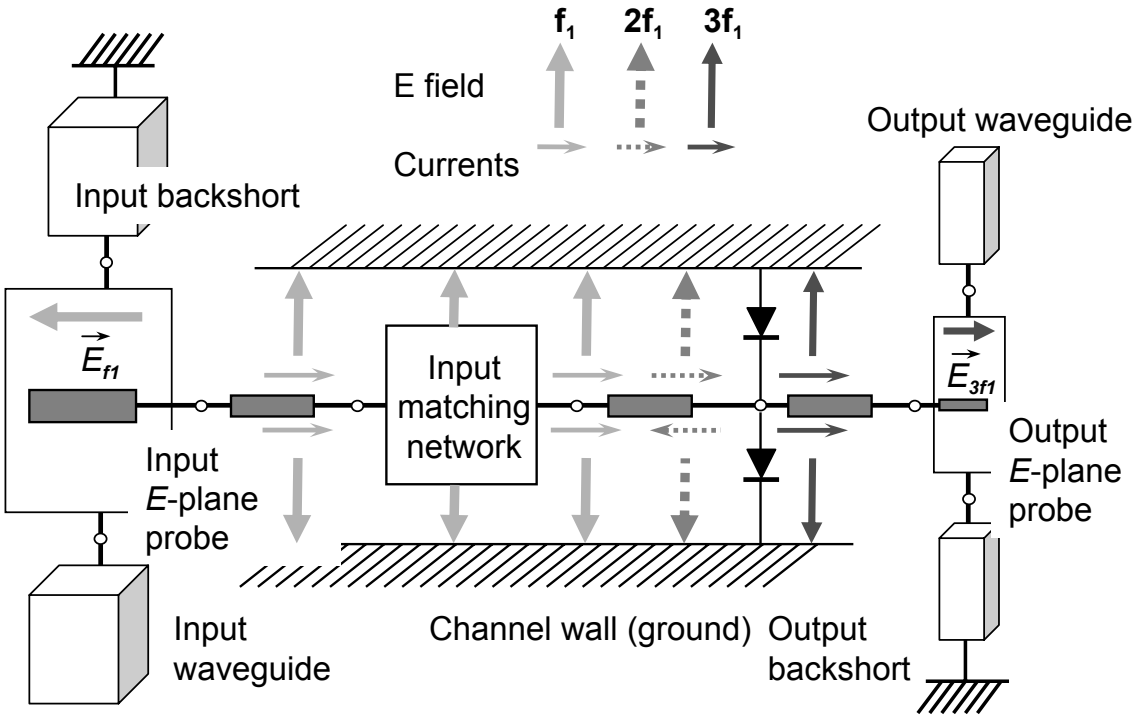


Figure 69: Block diagram of a 2-anode 900 GHz balanced tripler. The tripler uses a split-block waveguide design. The diodes are connected in series at dc and are in a balanced configuration at RF. The chip is inserted in a channel between the input and the output rectangular waveguides. An E-plane probe located in the input waveguide couples the signals at the fundamental frequency to a suspended microstrip line that can propagate only in a quasi-TEM mode. This line has several sections of low and high impedances used to match the diodes at the input and output frequency and to prevent the third harmonics from leaking into the input waveguide. The third harmonic produced by the diodes is coupled to the output waveguide by the second E-plane probe. Additional waveguide sections of different impedances and lengths (not shown) are used for the input and output matching. $\vec{E}_{f1}$ and $\vec{E}_{3f1}$ stand respectively for the electric field at the fundamental frequency f1 and at the output frequency 3×f1. The electric fields and the current lines are represented for the fundamental frequency f1 (thick light lines), the idler frequency 2×f1 (dashed lines) and the output frequency 3×f1 (light plain lines)

used in the anti-parallel configuration [124], enabling the generated odd harmonics to flow toward the same direction as the RF ground. The generated even harmonics proceed towards the opposite direction and are trapped in a virtual loop that consists of the two paths from the suspended microstrip line to the RF ground. Figure 70 shows this anti-parallel configuration, the virtual loop for the even harmonics, and the

termination loop for the odd harmonics. The RF ground of the diodes in Figure 70 is the metalized chip channel. The balanced configuration has worked well for making an efficient tripler with relatively wide bandwidth [124] at lower frequencies.

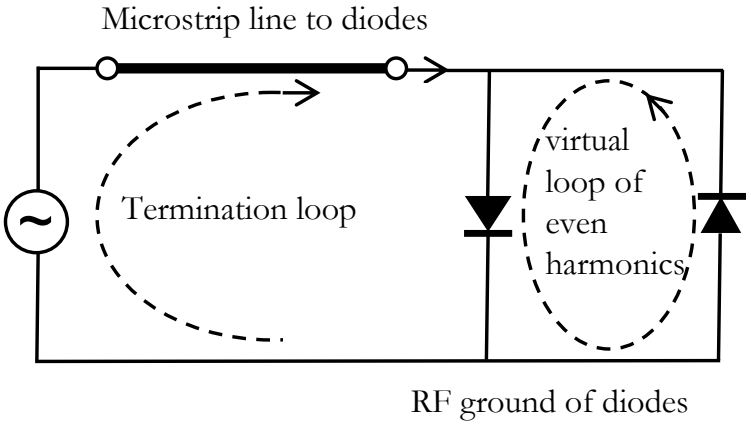


Figure 70: The anti-parallel configuration of diodes.

The E-plane probe in the input waveguide is used to couple the fundamental signal to the microstrip line on the GaAs chip. The chip channel housing the 900 GHz tripler chip has a crosssection of 95 μm by 65 μm and works as a metal shield and the outer conductor of the microstrip line that supports the TEM mode propagation for the odd harmonics. The low-impedance and high-impedance microstrip lines after the input probe are for the impedance matching of the diodes and a low-pass filter to block the high-order harmonics from leaking back into the input waveguide. Ideally, the generated 2^{nd} order harmonic is trapped in the virtual loop if the geometry of the diodes is perfectly symmetrical. In reality, the even harmonics leak out from the virtual loop due to the asymmetric geometry, yet they are kept from the output waveguide because of the cut-off frequency of the output waveguide is designed to be higher than the 2^{nd} harmonic. The diodes are placed close to the output E-plane probe to reduce RF losses and improve the matching at the output frequency. The generated 3rd harmonic is coupled to the output waveguide, followed by a horn antenna at the end to radiate the 3^{rd} harmonic power out. Figure 71 depicts the drawing of half

of the entire 900 GHz tripler. The chip was fabricated on a GaAs substrate with a thickness of 3 μm at the Jet Propulsion Laboratory. The entire tripler chip is elevated in the air after the assembly through the four metal beamleads on the chip. The input E-plane probe is on top of the GaAs substrate. By fabricating the chip on a thin membrane unwanted substrate modes are eliminated and dispersions and RF losses are reduced.

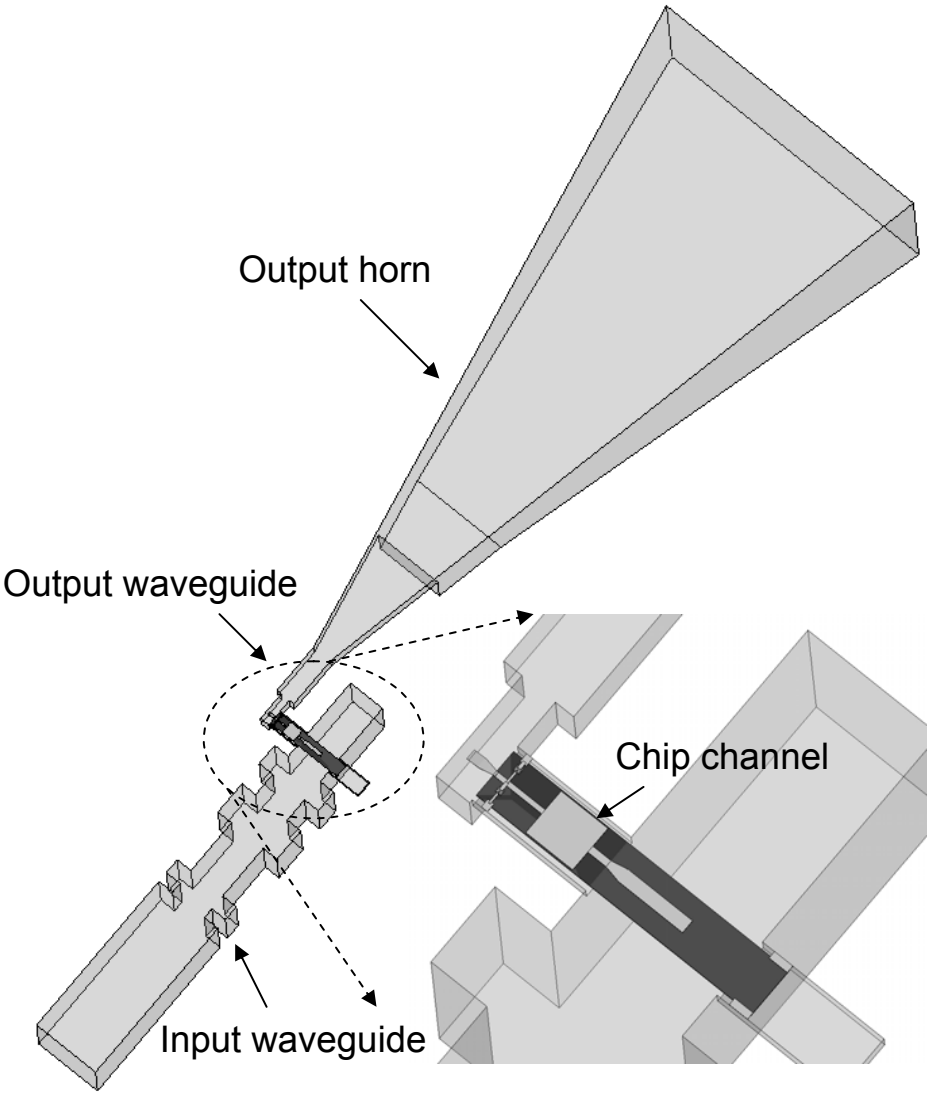


Figure 71: The drawing of half of the entire 900 GHz frequency tripler. The waveguide structure is cut along the E-plane center.

8.2.2 Waveguide Structure Design

Once the diode cell and size of the anodes has been optimized, the waveguide circuit is designed around this to optimize performance. Therefore, the height of the chip channel and the length of the backshorts are first optimized to maximize the coupling at the center frequency. The input signals are coupled to the suspended microstrip line that supports the propagation in the TEM mode. The transition that is optimized to maximize the coupling at the center frequency doesn't guarantee a wide bandwidth because the impedance of a waveguide is frequency-dependent. Then, an eight-section waveguide matching network is employed to extend the bandwidth without lowering the output power. The same procedure is used to design the output coupling and waveguide structure. The dimensions of the channel that runs between the input and the output waveguides are set to cutoff the first TE mode of the suspended microstrip line at the second harmonic, i.e. only a quasi-TEM mode is allowed to propagate inside this channel at the input frequency and at the idler frequency; therefore the second harmonic cannot propagate [122].The third harmonic propagates in the TEM mode in the chip channel and is coupled to the output waveguide through the output E-plane probe. During the circuit design special consideration is given to maintaining equal input coupling between the two anodes, and this is necessary to avoid over heating and diode burnout. The design topology, developed by Dr. Hui Wang and shown in Figure 72, is adopted in the design of the 828-963-GHz Two-anode Frequency Tripler [125].

8.2.3 The 900 GHz Membrane Chip

The purpose of the 900-GHz membrane chip is to provide a low-power source for pumping Superconductor-Insulator-Superconductor (SIS) and Hot Electron Bolometer (HEB) mixers. A unique feature of this chip is that almost all of the GaAs

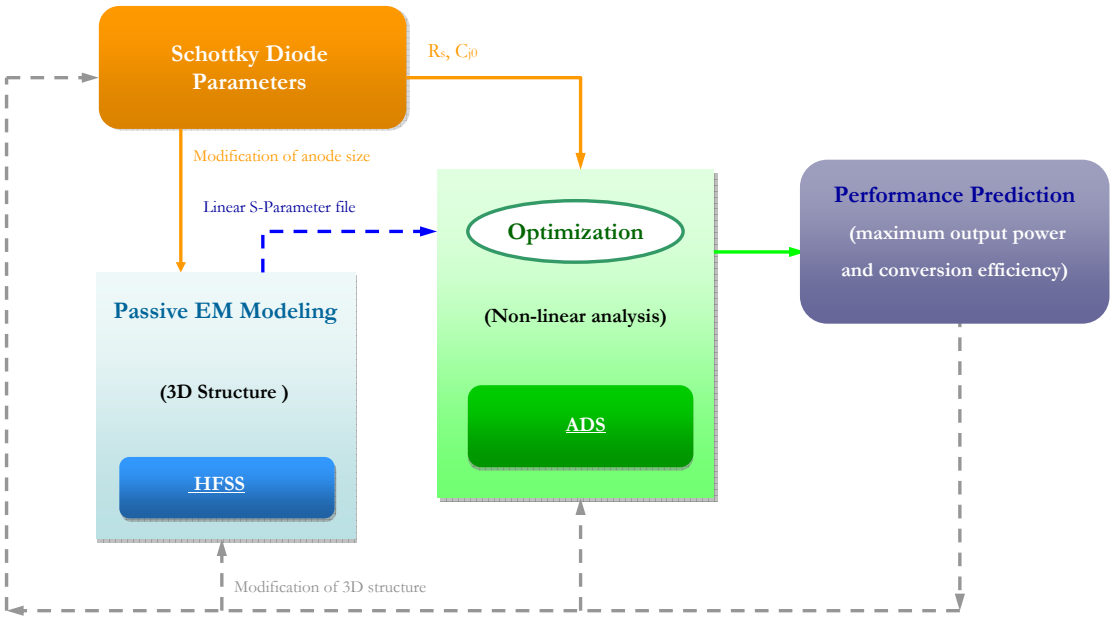


Figure 72: The design methodology of the frequency tripler [125].

substrate is removed, leaving only a 3-μm-thick membrane to support the circuits including diodes, probes, and impedance matching circuits. Monolithically integrated metal beam leads provide easy handling and support for the chip, along with the RF return for diodes. The entire chip can be simply dropped in the chip channel without the use of solder or epoxy. The simplicity of the entire chip layout makes the integration with waveguide circuits significantly easy and highly repeatable.

A simplified model of the Schottky diode is reported in [126], including a junction capacitance C_j in parallel with a conductance and in series with a resistance R_s. The series resistance consists of all impedance between the depletion region and the ohmic contact, including the epilayer resistance, the dc series resistance of the substrate, and the ohmic contact impedance [127]. The measured series resistance at dc is about 35 ohms per diode for this chip. The dc measurement of the series resistance, used as a figure of merit of the diodes and reported in [122] and [127], is not enough to represent the impedance at THz frequencies where skin effects and saturation effects cannot be ignored. Based on previous RF measurements, the series resistance used in our ADS

simulations needs to be increased to 50 Ohms. The junction capacitance classically modeled in [126] is a function of the junction area, semiconductor permittivity, and thickness of depletion layer that is determined by the doping of semiconductor epilayer and the built-in potential. With the increase of operating frequency, the size of anode becomes smaller. As a result, the junction capacitance becomes smaller, but with higher series resistance. An accurate three-dimensional model of the diode is drawn in HFSS, as shown in Figure 73 and simulated to take into account parasitic capacitances. The parameters of the diodes are given in Table 6.

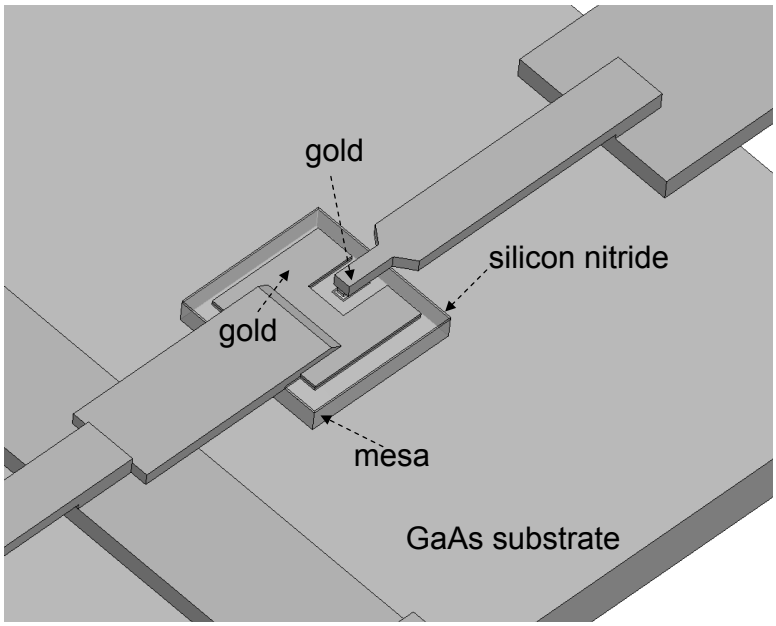


Figure 73: The three-dimension model of the Schottky diode.

8.2.4 The Micromachined Submillimeter-wave Antenna

The corrugated horn is the preferable antenna at these frequencies. Such horns have been demonstrated using laser chemical etching of silicon as shown in [111]. Similarly, the diagonal horn also provides acceptable performance for the purpose of pumping mixers but also requires a rather complicated process sequence for fabricating with the DRIE technology. We have incorporated a rectangular horn with the multiplier

Table 6: Physical and parameters and doing parameters of the JPL 900 GHz balance tripler.

Physical and electrical parameters	
Anode width	0.4 μm
Anode length	1.4 μm
Epilayer doping	5×10^{17}
GaAs thickness	3 μm
C_j	1.6 fF
R_s at DC	35 Ω

circuit. While this is not the optimum antenna structure it allows us to measure the performance of the multiplier. This horn consists of a machined slope in the fixture and a micromachined silicon part including the waveguide feed, transition and aperture. Figure 74 (a) gives half of the horn split along the E-plane center. Figure 74 (b) depicts that the silicon part is on top of the fixture. Figure 74 (c) shows the silicon part only.

The variable parameters in the design of horn are the flare angle θ, the thickness of the silicon t, the opening of the aperture a and b, and the length d. The horn, following the output waveguide of the tripler, has a cross section of 110 μm by 230 μm. The overall dimensions of the horn were initially chosen so that the horn would behave like a rectangular horn. A full-wave simulation was performed using Ansoft's HFSS. The horn has the aperture of 2200 μm by 1676 μm. Table 7 shows the optimized parameters of the horn. Figure 75 gives the far-field patterns of the horn, showing H-plane peak copolarized sidelobes 17 dB down from the pattern peak and E-plane peak copolarized sidelobes 10 dB down from the pattern peak. The 3-dB half-beamwidth is 10°.

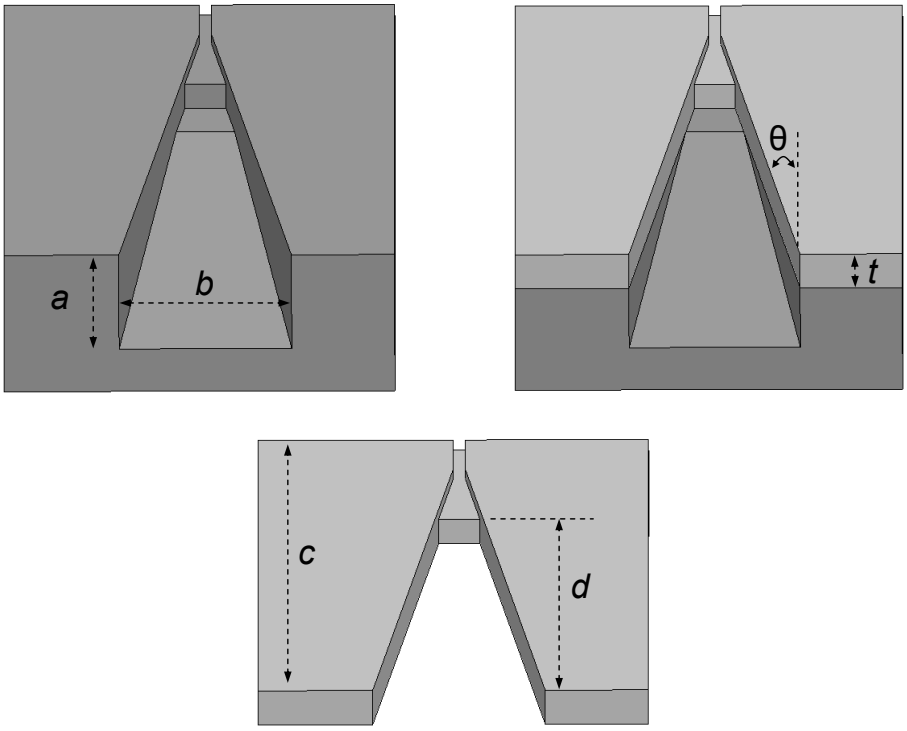


Figure 74: The depiction of the micromachining process used to form the horn: (a) half of the horn split along the E-plane center; (b) silicon part on top of the fixture; (c) silicon part only.

Table 7: Optimized dimensions of the 900 GHz micromachined antenna.

Dimensions	**Vaule (μm)**
a	1100
b	1676
c	4323
d	3123
t	400
θ	11.5°

8.3 Fabrication and Assembly of the Compact Waveguide Circuits

The deep reactive ion etching technique has been reported in [117] to fabricate millimeter-wave components. A similar process is employed here to fabricate the

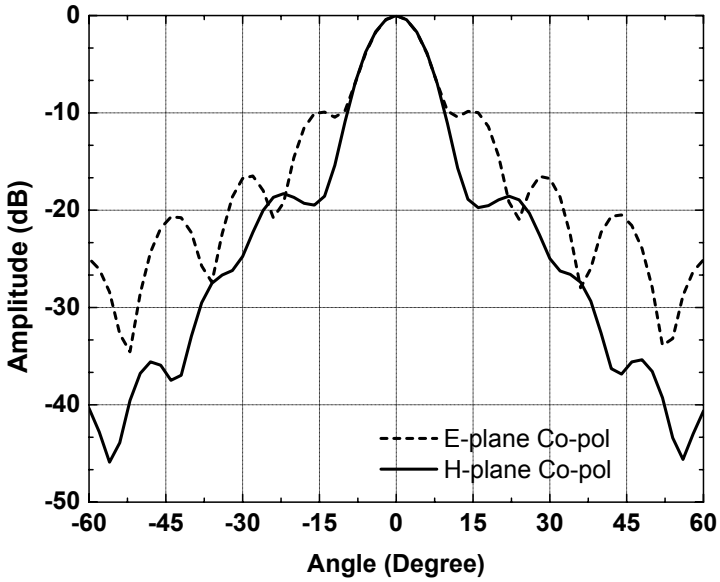


Figure 75: The simulated far-field patterns of the 900 GHz micromachined horn.

waveguide structure for the 900 GHz tripler. The first step is to rinse low resistivity silicon wafers (10-20 ohms-cm) and remove the organic residues. A layer of silicon dioxide is deposited on both sides of the wafer using a plasma-enhanced chemical vapor deposition process. Then, a photoresist layer is spun and patterned on the silicon dioxide layer. The exposed silicon oxide layer is etched away using a dry-etching technique. The patterned silicon is etched using the deep reactive ion etching with the BOSCH process. After that, the silicon substrate is flipped over and the process is repeated starting from the spinning of the photoresist. The micromachined samples are released after the removal of the silicon dioxide. A 3-μm-thick metal layer of Ti/Cu/Au is sputtered to form the metalized inner surfaces of waveguide structures. The SEM images of the waveguide circuits and the dimensional sensitivity analysis are given in Section IV in detail.

The fabricated silicon circuits are aligned through two alignment pins and mounted on the fixture with the tripler chip in turn mounted on the Si pieces. The tolerance of the fixture fabricated using direct machining is about 75 microns. A UG-387

waveguide flange forms at the input port of the fixture, as shown in Figure 76. The tripler chip in the micromachined waveguide structure is shown in Figure 77. The output of the fixture is the aperture of the horn antenna. The tolerance on the flange and alignment pins will result in the reflection of input power. A useful analysis of the waveguide flange misalignment can be found in [131] on a W-band waveguide. According to this analysis, the misalignment in the height direction is worse than that in the width direction for the same amount of misalignment over most of the interested frequency range.

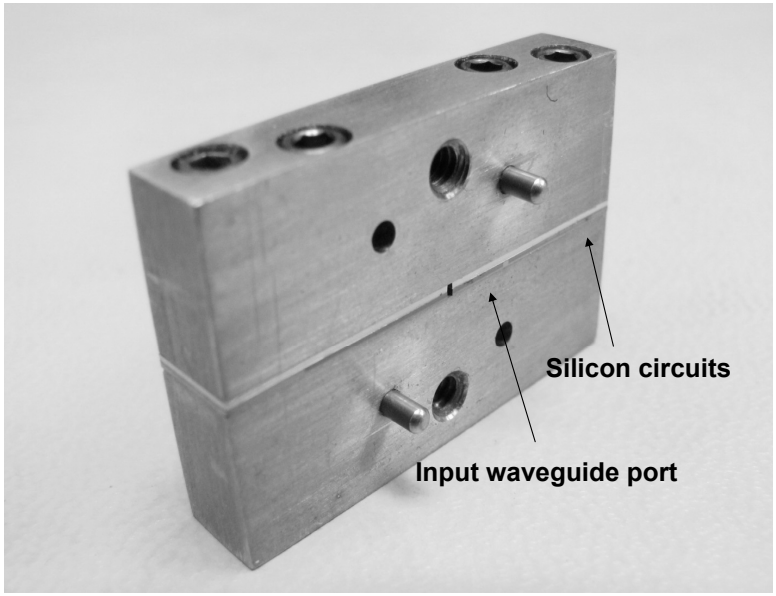


Figure 76: The fixture and the silicon circuits for measurement. A UG-387 waveguide flange forms at the input waveguide.

8.4 Measurement and Analysis

8.4.1 Measurement Setup

The measurement setup used for characterizing this 900 GHz tripler is shown in Figure 78. A commercial synthesizer source in the W-band is amplified via W-band power amplifiers. An attenuator, coupler and isolator are used before this signal is used to drvie a broadband 300 GHz tripler [132]. The isolator is calibrated and the

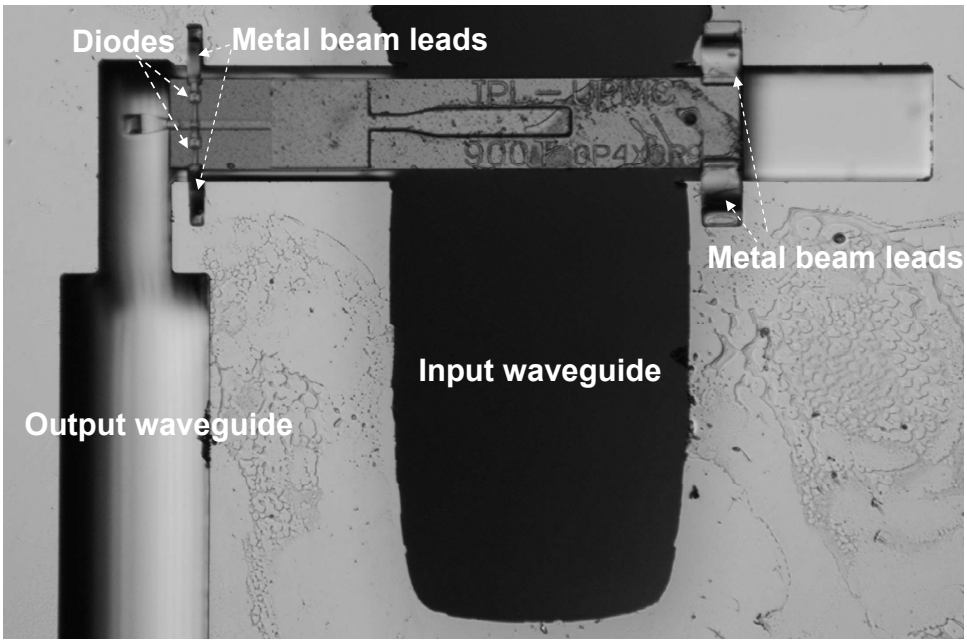


Figure 77: The tripler chip in the micromachined waveguide structures. The metal beam leads on the THz chip greatly improve the chip handling and make the assembly highly repeatable.

attenuator is used to provide a constant 100 mW input signal to the 300 GHz tripler. This tripler outputs 5-10 mW from 276 to 321 GHz.

The output power of the 900-GHz tripler was measured using a one-inch long circular to WR10 waveguide transition, a one-inch long WR10 waveguide section, and a PM2 Erickson Instruments power meter. As the 900-GHz tripler block was assembled by clamping the waveguide transition directly onto the output face of the tripler block, measurements of the output power of the 900-GHz tripler were not corrected for losses in the waveguide transition and straight sections. The 900-GHz tripler output power was measured in the 837-963 GHz band every 4.5 GHz. The bias voltage of the 300-GHz tripler was optimized at each frequency to obtain maximum power. Conversion efficiencies were calculated by dividing the power levels recorded at the output of the 900 GHz chain by the power levels previously recorded at the output of the driver stage.

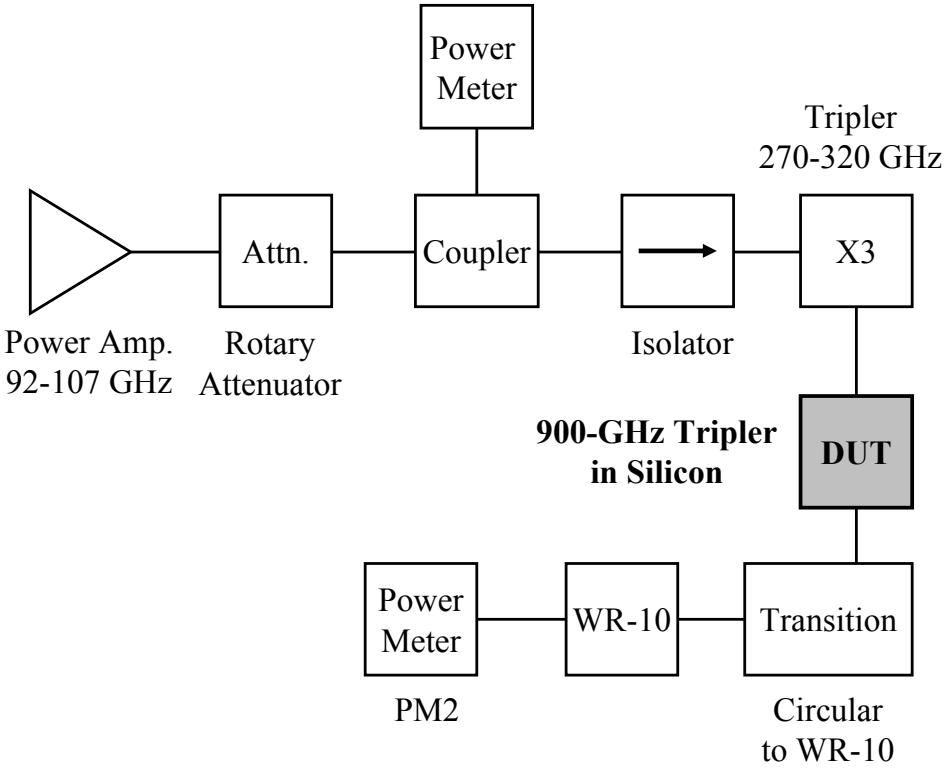


Figure 78: The measurement setup. From the left to the right, the measurement chain consists of a W-band power amplifier, a rotary vane attenuator, a W-band coupler, an isolator, a WR10 waveguide, a JPL in-house 300-GHz tripler, the 900-GHz tripler, a circular to WR10 transition, a WR-10 waveguide, and a PM2 power meter.

8.4.2 900 GHz Multiplier Frequency Response

The measured output power and the measured efficiency of the 900 GHz tripler are shown in Fiugre 79. At room temperature, the measured output power was 23.7 μW to 85.3 μW from 828 GHz to 963 GHz and was above 60 μW from 877.5 GHz to 922.5 GHz. The input power generated by a 300 GHz tripler was 8.34 mW to 9.86 mW from 276 GHz to 321 GHz. In the estimated responses, the additional loss from the surface roughness, reentrant angle, and silicon brim discussed below in detail is considered as well as a total 1.5-dB de-embeded loss for the mismatching at input flange and output, circular to WR-10 transition, and a 1-inch-long WR-10 waveguide. However, no corrections have been made to the measured output power numbers.

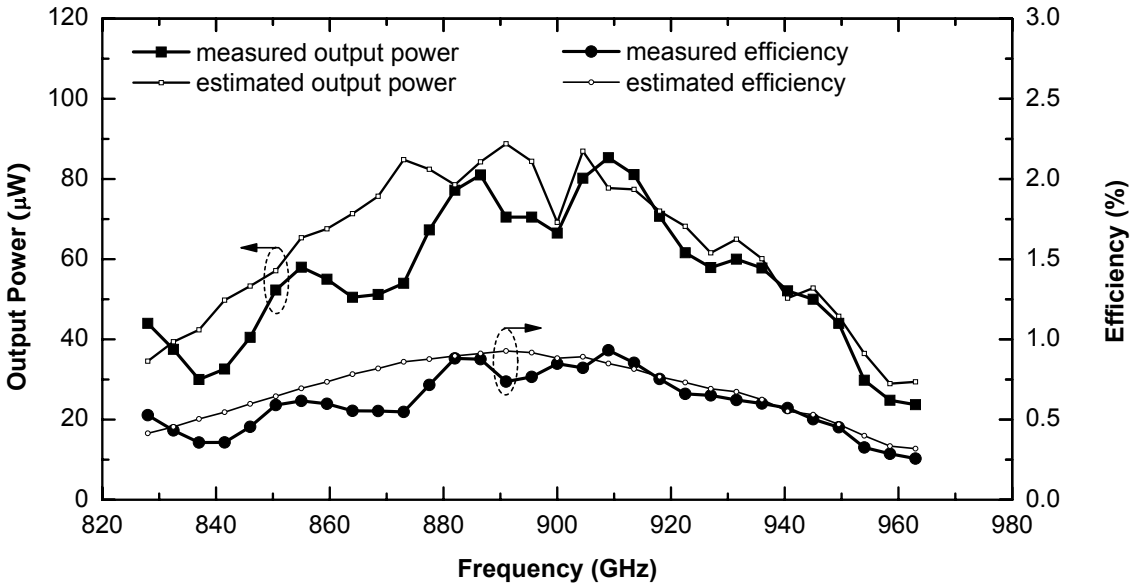


Figure 79: The estimate and measured output power and efficiency at room temperature. No corrections have been made to the measured output power and efficiency numbers. At room temperature, the measured output power was 23.7 μW to 85.3 μW from 828 GHz to 963 GHz.

8.4.3 Dimensional Sensitivity Analysis

Precision tolerances in the fabrication are vital to the THz frequency multipliers because the operating wavelength is on the order of 300 μm at 900 GHz. Figure 80 shows the SEM images of the silicon waveguide structures, including output horn in Figure 80(a), an input waveguide in Figure 80(b), a cross section of the waveguide structure with the slope angle less than 2° in Figure 80(c) and the surface roughness more than 1 μm in Figure 80(d).

Several tolerances in the fabrication are considered in this design. First, tolerances exist in the mask layer used for dry etching. The mask layer, e.g. positive photoresist, has a taper profile towards the sidewall, which means the thickness of the positive photoresist is thinner on the edge than expected. The photoresist on the edge is etched away first in a long etching process due to the limited selectivity, then the photoresist-protected substrate is exposed and etched eventually. This phenomenon leads to a wider opening of the etched features but can be compensated through

mask design. Second, tolerances from the deep reactive ion etching process normally consist of the vertical striation and the reentrant angle. To reduce these tolerances, the fabrication recipe is optimized by tuning many factors, including the pressure in an etching chamber, the flow rate of gases, the time for etching and passivation, the power of etching and passivation, and the exposed area of silicon. Our process has been optimized to provide near 90° sidewalls.

The vertical striation worsens the surface roughness on the sidewall. In the THz range, the current distributes itself near the surface of a transmission line due to the skin effect. The surface roughness increases the total current path and leads to an increase in conductor loss, which is usually computed by [130]:

$$\frac{\alpha_c}{\alpha_{c0}} = 1 + \frac{2}{\pi}\tan^{-1}\left(1.4\left(\frac{\triangle}{\delta}\right)^2\right) \tag{10}$$

where $\triangle/\delta$ is the normalized rms roughness. The conductor loss α_{c0} can be estimated using a full-wave simulator, e.g., HFSS. The skin depth of gold is about 120 nm at 300 GHz and the estimated rms roughness on sidewall is more than 1 μm, as shown in Figure 80(d). Therefore, the increased conductor loss is about 0.02 dB per wavelength at 300 GHz and 0.04 dB per wavelength at 900 GHz. As a result, an additional 0.7 dB conductor loss comes from the surface roughness for the input waveguide, output waveguide, and horn.

Different from the vertical striation, the reentrant angle caused by the lack of passivation on the sidewall in the etching cycle leads to an impedance mismatch because of the deformation of the cross section. The effect of reentrant angle is worse with the increase of etching depth. The fabrication recipe is first optimized to minimize the reentrant angle. In addition, this tolerance is treated carefully in the design and simulations to avoid degrading the performance substantially, especially for the input waveguide structure that has the maximum depth.

Besides the vertical striation and reentrant angle, the bottom of a dry-etched

waveguide is hard to make flat, as shown in Figure 80(c) in this chapter and Figure 8 in [116]. This non-flat bottom results in a thin silicon brim left on the waveguide at the end of the process when the silicon wafter is etched through. The silicon brim is only a few microns thick and thus fragile enough to be broken by strong nitrogen flow, leaving an irregular shape after the cleaning process. To further evaluate the tolerances of the reentrant angle and the irregular shape, the input waveguide structure is scanned and a 3-D model is built to represent these tolerances. The estimated additional loss is about 0.65 dB using the simulation of Ansoft's HFSS and Agilent's ADS.

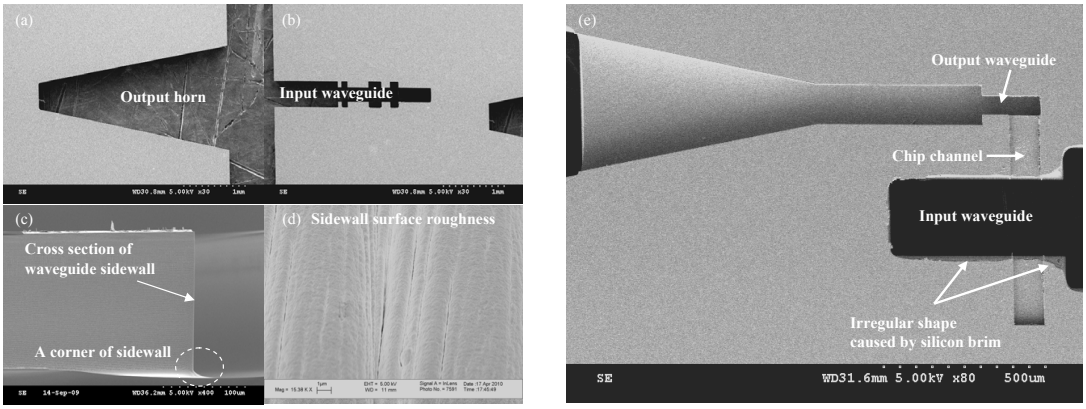


Figure 80: SEM images: (a) output horn; (b) input waveguide; (c) cross section of waveguide sidewall; (d) surface roughness on sidewall; (e) the input and output backshorts as well as the chip channel.

8.4.4 Power Sweep

The power sweep measurement was made at the frequency with the highest output power. With the attenuator fully open and 150 mW driving the 300-GHz tripler, a maximum power of 121.6 μW was recorded at 891 GHz. As the attenuator is gradually closed, the output power of the 900-GHz tripler was recorded along with the power measured at the W-band coupled port. The bias voltage of the 300-GHz tripler was adjusted to get optimum output power at each point. To find the input power going into the 900-GHz tripler, the last stage of the tripler was removed from

the measurement setup. The Erickson Instruments power meter and a WR-10 to WR-3 waveguide transition was then attached to the 300-GHz tripler, and the power at each point was measured by adjusting the attenuator until the W-band coupled port power matches the previously recorded values, and the bias voltage of the 300 GHz matches the previously set values. Conversion efficiency was calculated in the same way as was done in the frequency sweep. Figure 81 depicts the measured Pin-vs-Pout at the frequency of 909 GHz for both output power and conversion efficiency.

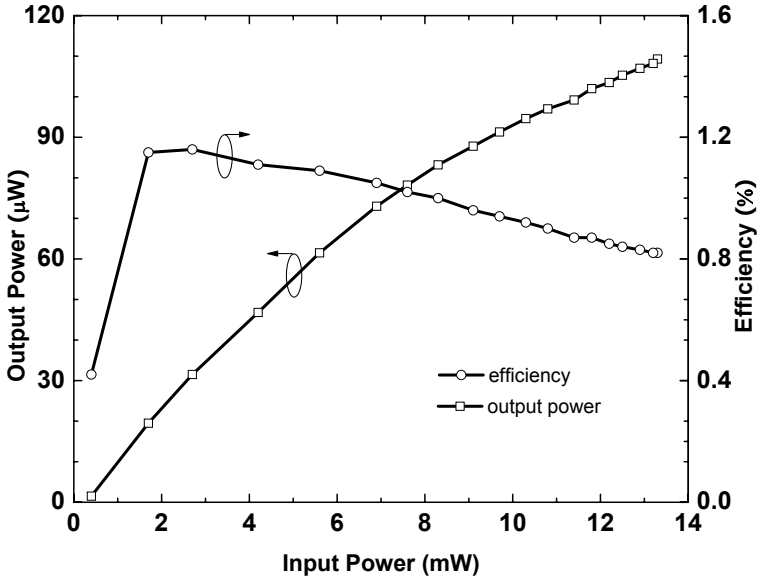


Figure 81: The measured output power and measured efficiency v.s. input power at 909 GHz.

8.5 Conclusion

In the last two decades, the design of the THz multipliers and the fabrication of diodes and chips had made extraordinary progress. In this work, silicon micromachined waveguide structures are successfully integrated, for the first time to the best knowledge of the authors, seamlessly with THz chips at such high frequencies in both the design and the measurement. This research result enables the silicon micromachining technique to build low-loss and low-cost THz signal sources. The tripler

provides state of the art performance, 23.7 μW to 85.3 μW from 828 GHz to 963 GHz and more than 60 μW from 877.5 GHz to 922.5 GHz, in a compact structure at room temperature. Successful demonstration of this technology can now open up the possibilities of using this approach for building multi-pixel heterodyne array receivers for future applications.

CHAPTER IX

THE CONTRIBUTIONS AND PUBLICATIONS TO DATE

This thesis explored the design, simulation, fabrication, and characterization of micromachined millimeter-wave modules and signal source for submillimeter-wave output. The primary contributions are summarized as the following items:

- The low-loss micromachined meander waveguide and filter
- The low-loss hybrid and power divider
- The novel low-loss CPW-to-waveguide transition and filter
- The novel high-Q 60 GHz cavity-based tunable resonator and filter
- The first 900 GHz frequency multiplier using silicon micromachined waveguides

This work in my Ph. D. study has led to the following publications:

9.1 Journal Publications

- Yuan Li, Pete L. Kirby, Olivier Offranc, and John Papapolymerou, "Silicon Micromachined W-band Hybrid Coupler and Power Divider Using DRIE Technique," IEEE Microwave and Wireless Components Letters, Vol. 18, No. 1, pp 22 - 24, Jan. 2008.
- Yuan Li, Bo Pan, Cesar Lugo, Manos Tentzeris, John Papapolymerou, "Design and Characterization of a W-Band Micromachined Cavity Filter Including a Novel Integrated Transition From CPW Feeding Lines," IEEE Transactions on Microwave Theory and Techniques, Vol. 55, No. 12, pp. 2902-2910, December 2007.

- Bo Pan, Yuan Li, Manos M. Tentzeris and John Papapolymerou, "Surface Micromachining Polymer-Core-Conductor Approach for High Performance Millimeter-Wave Air-Cavity Filter Integration," IEEE Transactions on Microwave Theory and Techniques, Vol. 56, No. 4, pp. 959-970, April 2008.

- Bo Pan, Yuan Li, Manos M. Tentzeris and John Papapolymerou, "A High-Q Millimeter-Wave Air-lifted Cavity Resonator on Lossy Substrates," IEEE Microwave and Wireless Components Letters, Vol. 17, No. 8, pp 571 - 573, Aug. 2007.

- Bo Pan, Yuan Li, George E. Ponchak, Manos M. Tentzeris and John Papapolymerou, "A Low-loss Substrate-Independent Approach for V-band Transceiver Front-end Integration using Micromachining Technologies," IEEE Transactions on Microwave Theory and Technique, Vol. 56, No. 12, pp. 2779-2788, December 2008.

- Stanis Courreges, Yuan Li, Zhiyong Zhao, Kwang Choi, Andrew Hunt, Stephen Horst, John D. Cressler, and John Papapolymerou "A Ka-Band Ferroelectric Tunable Filter," IEEE Microwave and Wireless Components Letters, Vol. 19, No. 6, pp. 356-358, June 2009

- Stanis Courreges, Yuan Li, Z. Zhao, K. Choi, A. Hunt, J. Papapolymerou, "A Quasi-Elliptic Ferroelectric Tunable Filter for X-Band Applications," IEEE Microwave and Wireless Components Letters, Vol. 19, No. 4, pp. 203-205, April 2009.

- Stanis Courreges, Yuan Li, Z. Zhao, K. Choi, A. Hunt, J. Papapolymerou, "Two-pole X-Band-Tunable Ferroelectric Filters with Tunable Center Frequency, Fractional Bandwidth, and Return Loss," IEEE Transactions on Microwave Theory and Techniques, Vol. 57, No. 12, pp. 2872-2881, December 2009.

9.2 Conference Publications

- Yuan Li, Bo Pan, Manos M. Tentzeris, John Papapolymerou, "A Fully Micromachined W-Band Coplanar Waveguide to Rectangular Waveguide Transition," 2007 IEEE International Microwave Symposium, pp. 1031 - 1034, Jun. 2007.

- Pete L. Kirby, Yuan Li, Qun Xiao, Jefferay Hesler, John Papapolymerou, "Silicon Micromachined Multiplier Utilizing Heterostructure Barrier Varactor Diode," 2007 IEEE International Microwave Symposium, pp. 1141 - 1144, 3-8 Jun. 2007.

- Yuan Li, P. L. Kirby and J. Papapolymerou, "Silicon Micromachined W-Band Bandpass Filter Using DRIE Technique, 2006 IEEE European Microwave Conference, pp. 1271-1273, Manchester, Sep. 2006.

- Yuan Li, Pete L. Kirby and John Papapolymerou, "Silicon Micromachined W-Band Folded and Straight Waveguides Using DRIE Technique, 2006 IEEE/MTT-S International Microwave Symposium Digest, pp. 1915-1918, San Francisco, CA, Jun. 2006.

- S. Courreges, Yuan Li, Z. Zhao, K. Choi, A. Hunt, J. Papapolymerou, "Ferroelectric Tunable Bandpass Filters for Ka-Band Applications, 2008 IEEE European Microwave Conference Digest, pp. 56-58, 2008

- Bo Pan, Yuan Li, M.M.Tentzeris and J.Papapolymerou, "A Novel Low-loss Integrated 60 GHz Cavity Filter with Source-Load Coupling using Surface Micromachining Technology", 2008 IEEE-IMS Symposium, pp. 639-642, Atlanta, June 2008.

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